Digital Equipment Corporation
Maynard, Massachusetts

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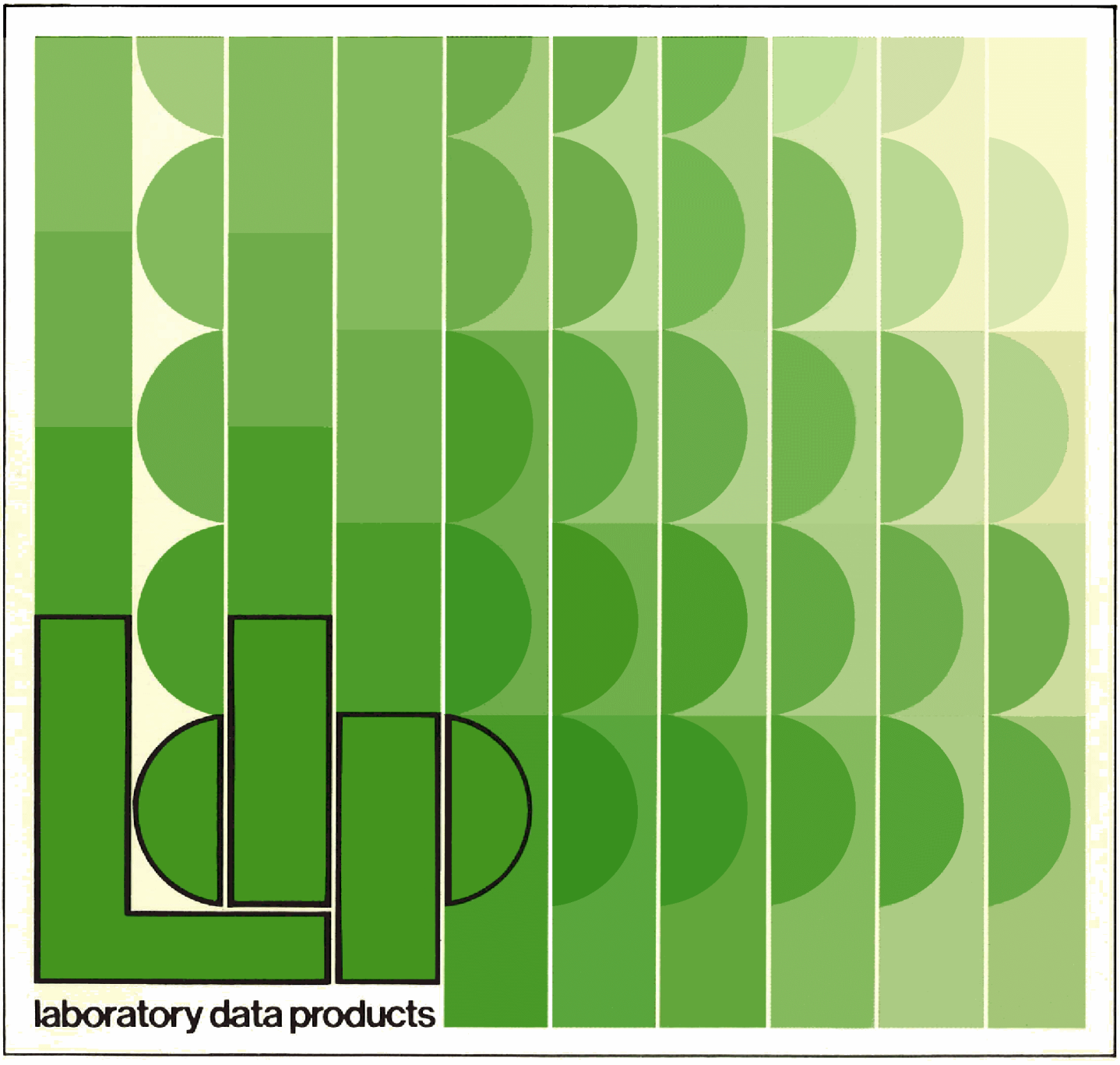
LPS11-S laboratory peripheral system maintenance manual



DEC-11-HLPMA-B-D

LPS11-S laboratory peripheral system maintenance manual

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

The LPS11-S Laboratory Peripheral System is a high-performance, modular, real-time subsystem that interfaces with the PDP-11 family of computers via a single asynchronous bus, the Unibus. The flexibility of the LPS11-S makes it well suited to a variety of applications in general laboratory operation, including biomedical research, analytical instrumentation, data collection and reduction, monitoring, data logging, industrial testing, engineering, and technical education.

The basic LPS11-S comprises the Unibus interface, front and back access panels, prewired slots for modular plug-in options, and a power supply, all housed within a single cabinet, which can be operated either mounted in a cabinet rack or placed upon a desk or table (Figure 1-1).

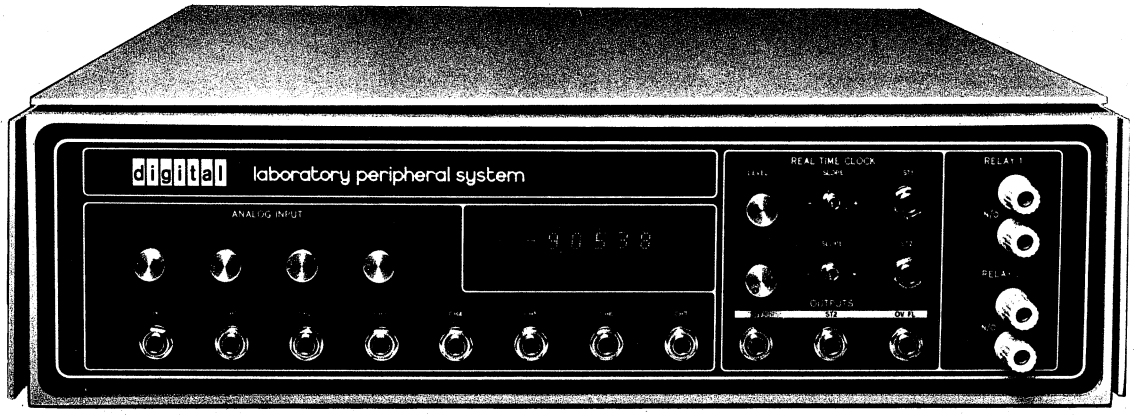

Figure 1-1 LPS11-S Laboratory Peripheral System

The plug-in options are defined in relation to the LPS11-S, and not to the PDP-11 Unibus. The basic system can be expanded to contain a 12-bit, 16-channel analog-to-digital system with direct memory access and dual sample-and-hold capabilities and a six-digit numeric light-emitting diode (LED) readout. A real-time programmable clock, a digital input/output interface, and a scope control can be added to make a complete LPS11-S system.

1.2 SCOPE

This manual provides sufficient installation, theory of operation, programming, and maintenance information to enable the user to operate and maintain the LPS11-S Laboratory Peripheral System. Chapter 1 introduces and describes the LPS11-S on a block diagram level and provides specifications for the basic unit and its options.

Chapter 2 deals with the various aspects of installation that pertain to the LPS11-S and each of the available options.

Chapter 3 discusses the theory of operation for the benefit of the LPS11-S user and maintenance personnel. Operation of each subsystem or unit is described from a block diagram and a detailed circuit analysis point of view. Such description presupposes that the reader is familiar with DEC logic and the PDP-11 family of processors.

Chapter 4 describes the various adjustments and calibrations that might be required in the maintenance of the LPS11-S, while Chapter 5 contains reference information necessary for system troubleshooting.

Programming information in this manual is limited to the level required for system maintenance. For detailed information regarding programming, refer to the appropriate manual from the related documentation listed in Table 1-1. Information about other PDP-11 equipment is also available in that list of documentation.

Table 1-1
Related Documentation

Document Title	DEC Document No.
LPS11-S Laboratory Peripheral System User's Guide	DEC-11-HLPGA-A-D
PDP-11 Peripherals Handbook	DEC, 1973-74
LPS11-S Laboratory Peripheral System Engineering Drawings	Refer to DEC Drawing No. D-DI-LPS11-0-0.

1.3 BLOCK DIAGRAM DISCUSSION

Figure 1-2 is a block diagram of the LPS11-S Laboratory Peripheral System, together with the available options. The system communicates with the PDP-11 Unibus through the M7015 Unibus Interface module, which is referred to herein as the *bus control.*

1.3.1 Bus Control

The bus control decodes all option addresses, controls all interrupts and vector addresses, buffers the PDP-11 Unibus, and creates a secondary internal bus. The bus control is capable of controlling multiple interrupts, each with an assigned priority level. A vector address is associated with each interrupt. The first vector address is jumper-selectable; the remaining five vectors follow in sequence.

The various LPS11-S options are connected to the internal bus, as shown in Figure 1-2, and the bus control serves to buffer the Unibus from them so that the LPS11-S system package appears as a single unit load on the PDP-11 Unibus.

1.3.2 LPSAD-12 A/D Converter System Option

The LPSAD-12 A/D Converter enables the user to sample analog data at specified rates and store the equivalent digital value for subsequent processing. Sample-and-hold circuits ensure accurate A/D conversion of rapidly changing signals by holding the input voltage constant until the A/D conversion process is completed. A multiplexer permits the A/D converter to handle eight analog input channels, which are designated 0 through 7. Channels 0 through 3 are connected to phone jacks on the front panel and/or potentiometers that can be used to establish program parameters. The remaining four channels, 4 through 7, are only accessible via phone jacks on the front panel.

A six-digit LED display on the front panel can be used as a general-purpose programmable device to display A/D conversions, time readout of the real-time clock, processor address readouts, or a digital I/O status indication.

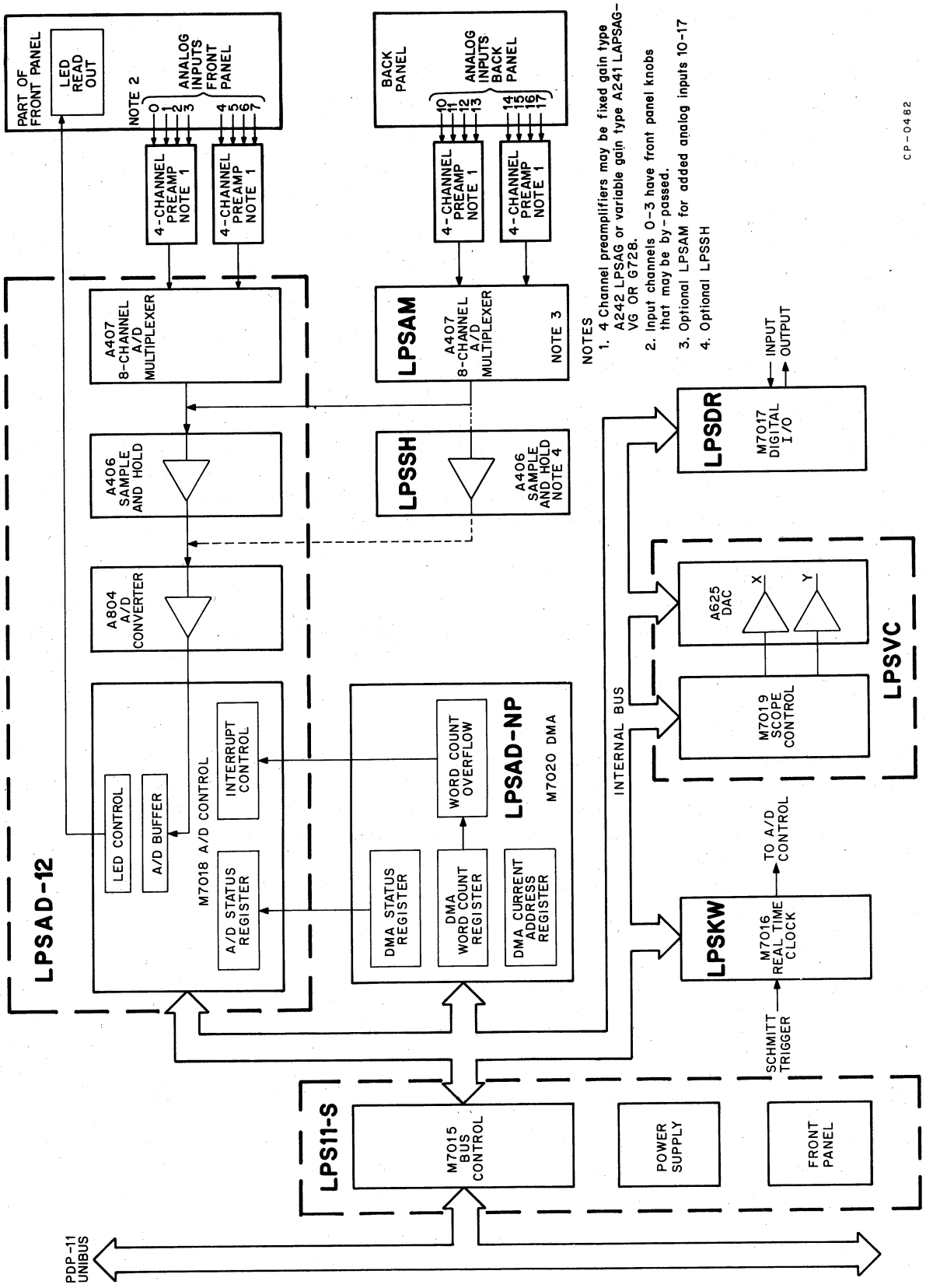

Figure 1-2 LPS11-S Laboratory Peripheral System and Options, Block Diagram

The following options are available with the LPSAD-12 A/D Converter system:

a. LPSAM 8-Channel Expansion Multiplexer – The LPSAM allows the system to be expanded to handle eight additional analog input channels. These channels, designated 10 through 17, are accessible at the rear panel.

b. LPSAD-NP Direct Memory Access (DMA) – The LPSAD-NP Direct Memory Access option allows the A/D conversions to be stored in memory at maximum rates without processor intervention.

c. LPSAG and LPSAG-VG Preamplifiers – The LPSAG 4-Channel Preamplifier option provides preamplifiers for four analog input channels that provide each channel with a ±1V differential input. The LPSAG-VG option provides additional ranges of 0 to 2V, ±5V, and 0 to 10V.

d. LPSSH Dual Sample-and-Hold – The LPSSH Dual Sample-and-Hold option allows the simultaneous acquisition of data from two predetermined channels.

1.3.3 LPSKW Programmable Real-Time Clock

The LPSKW Programmable Real-Time Clock option provides several methods of accurately measuring and counting intervals and events. It can be used to synchronize the central processor to external events, measure time intervals between events, provide interrupts at programmed intervals, or start analog-to-digital conversions with the overflow from the clock counter or the firing of a Schmitt trigger. Many of these operations can be performed concurrently.

1.3.4 LPSVC Display Control

The LPSVC Display Control option can operate with the DEC VR14 CRT Display or the VR20 Two-Color CRT Display, or with the Tektronix RM503, 602, 604, 611, or 613 Storage Display oscilloscopes. The LPSVC Display Control can produce a display in the form of a $4096_{10} \times 4096_{10}$ dot array. The display control offers four program-controlled modes of intensification.

1.3.5 LPSDR Digital Input/Output

The LPSDR Digital I/O option consists of a 16-bit buffered input register and a 16-bit buffered output register. Program control of input/output data is achieved in either of two selectable modes. The program transfer mode controls the transfer of data between the digital I/O registers and memory. The external interrupt mode allows an external device to initiate the transfer of data. Two programmable, normally-open relays provide a convenient means of controlling laboratory equipment.

1.4 SPECIFICATIONS SUMMARY

1.4.1 LPSAD-12 A/D Converter

Input Voltage Range:	±5V, single-ended
Input Channels:	8
Input Impedance:	$10^9\ \Omega$ in parallel with 100 pF, measured at rear panel
Input Bias Current:	
Channel on +10V input:	200 nA typical; channel on input clamps to ±10V
Channel off:	200 nA typical
Switching transient:	−5 mA maximum, 0.5 μs maximum

Resolution:	12 bits (1 part in 4096) can be reduced to 8, 9, 10, or 11 bits for faster conversion time with switch on module
Output Format:	Parallel, 12 bits, right-justified, offset binary, double-buffered
Accuracy at 25° C:	±0.035% of full scale
Linearity:	0.02% of full scale
Differential Linearity:	1 LSB
Temperature Stability:	30 ppm/° C (0.003%FS/° C)
Repeatability:	$2\sigma \leqslant 1/2$ LSB
Conversion Time:	20 μs time lapse from start command until a 12-bit result is acquired
Control:	Controlled by programmed instructions, clock counter overflow, or Schmitt trigger from LPSKW
Maximum Program Throughput Rate:	PDP-11/20 with optimal coding
Programmed Start:	40 kHz typical
Overflow or Schmitt trigger start:	45 kHz typical

1.4.2 LPSAM Multiplexer

Input Voltage Range:	±5V, single-ended
Input Channels:	8
Input Impedance:	10^9 Ω in parallel with 100 pF, measured at rear panel
Input Bias Current:	
Channel on +10V input:	200 nA typical; channel on input clamps to ±10V
Channel off:	200 nA typical
Switching Transient:	-5 mA maximum, 0.5 μs maximum
Analog Output Voltage Range:	±5V

1.4.3 LPSAG/LPSAG-VG Preamplifier

Input Voltage Range:	
LPSAG:	±1V differential
LPSAG-VG:	±1V, 0 to +2V, ±5V, 0 to +10V
Input Channels:	4

Input Impedance:	
+ to ground:	128K in parallel with 100 pF
- to ground:	64K in parallel with 100 pF
Differential:	128K in parallel with 50 pF
Input Bias Current:	40 nA maximum at + or - input
Common Mode Rejection:	60 dB at 0 to 60 Hz
Accuracy:	0.005% of full scale
Linearity:	0.005% of full scale
Analog Output Voltage Range:	±5V
Bandwidth:	
3 dB:	60 kHz
1 dB:	30 kHz
Full power:	4 kHz, ±5V output
Slew Rate:	0.3V/μs, typical

1.4.4 LPSKW Real-Time Clock

Input Voltage Range:	±5V, nominal
Input Type:	Differential
Input Impedance:	50K
Minimum Input Pulse Width:	2 μs square wave
Maximum Input Voltage:	±50 Vdc
Hysteresis:	0.3V, standard
Common Mode Rejection:	35 dB
Input Threshold:	Variable between ±5V
Slope:	+ and - switch-selectable
Output Voltages:	a. 0 to 5V – falling edge denotes firing of the Schmitt trigger; resets upon recrossing the threshold voltage for outputs 1 and 2
	b. Clock overflow; 0 to 5V
Maximum Frequency:	50 kHz
Minimum Input Voltage:	0.5V, peak-to-peak standard hysteresis

1.4.5 LPSVC Display Control

These specifications represent the standard configuration for the VR14 and VR20.

DAC Converter Specifications (Internal and External):

Output Voltage	±5V
Resolution:	1 part in 4096 (0.025% FS)
Absolute Accuracy:	0.1%
Slewing Speed:	10V/0.5 μs
Settling Time to 0.03%:	4 μs
Drive Capability:	300 ft at 50 pF/ft cable
Offset Adjustment:	200 mV
Gain Adjustment:	20 mV
Z Axis:	Z axis polarity is controlled by a jumper marked Z on the M7019 module. The setting of that switch determines whether the pulse is positive or negative.
Pulse Width:	1 μs
Pulse Size:	+4V to -2V
Rise Time:	100 ns
Fall Time:	200 ns

1.4.6 LPSDR Digital I/O

Control:	Controlled by programmed instructions
Input Register:	Protected to ±20 Vdc (recoverable protection only; circuits will have fuse-resistors for protection above 20 Vdc) Logical 1 = ground (0.4V maximum) Logical 0 = +3V (TTL logic) External inputs must be capable of sourcing a minimum 3.5 mA of current when a logical 1 is supplied
Output Register:	Protected to ±20 Vdc (recoverable protection only; circuits will have fuse-resistors to protect above 20 Vdc) Logical 1 = ground (0.4V maximum) Logical 0 = +3V (+5V maximum) Capable of sinking 30 mA and sourcing 10 mA

Input Control and Output Control:	1 μs typical, 200 μs minimum (driving capabilities depend on the characteristics of the particular cable being used; refer to the *LPS11 Laboratory Peripheral System User's Guide,* Figure 4-3, for instructions on calculating maximum cable lengths)
Relays:	5A resistive load @ 115 Vac
	2.5A resistive load @ 230 Vac
	Contact bounce 20 ms minimum

1.4.7 Power Supply

Input Voltage:	100V/115/230 Vac, single-phase
Input Frequency:	50–60 Hz +5%
Input Current:	3.0/2.5/1.25A rms
Input Power:	280W
Output 1:	
Voltage:	5 Vdc
Current:	0–13A
Line Regulation:	1% or 50 mV
Load Regulation:	2% no load to full load
Ripple:	Less than 50 mV p-p
Power Storage:	6 ms min @ full load + low line voltage
Temperature Coefficient:	-100 ppm/° C
Overvoltage Protection:	7.0 Vdc maximum, crowbar @ 5.7V
Outputs 2 and 3:	
Voltage:	+15 and -15 Vdc
Current:	2A each output
Line Regulation:	0.03%
Load Regulation:	0.03 no load to full load
Ripple:	5 mV p-p maximum
Voltage Sensing:	Remote, 2 wires per output
Temperature Coefficient:	+25 ppm/° C

LTC:

Frequency:	ac line 50/60 Hz
Output – High Voltage:	2.4V minimum 3.3V typical
Output – Low Voltage:	0.4V maximum 0.2V typical @ 16 mA

AC LOW and DC LOW:

Output – High Voltage:	3.5V minimum
Output – Low Voltage:	0.8V maximum @ 50 mA

1.4.8 LPSAM-SG/BA408 Switched Gain Multiplexer

Electrical

Input Channels	8 (single-ended)	
Switching	Break-before-make	
Input Range	±5 V	G=1
	±1.25 V	G=4
	±312.5 mV	G=16
	±78.125 mV	G=64
Gain Accuracy	0.02%	
Linearity	0.01%	
Input Impedance	10^9 in parallel with 0.01 μF	
Input Bias Current	±400 nA max., $-15\ V \leqslant V_{in} \leqslant +10\ V$	
Input Offset Voltage	Adjustable to zero	
Offset Drift	5 μV/° C max. RTI* + 120 μV/° C max. RTO*	
Bandwidth	100 kHz min., 150 kHz typ.	
Settling Time (to ±½ LSB)	15 μs max.	
Crosstalk	80 db min. at 1 kHz, 20 db/decade rolloff	
Noise (rms)	70 μV max. RTI* + 550 μV max. RTO*	
Warmup Time	3 minutes	

*RTI = referred to input
*RTO = referred to output

Power Requirements

+15 V ± 0.1% at 65 mA max.
−15 V ± 0.1% at 40 mA max.
+5 V ± 5% at 120 mA max.

Environmental

Operating Temperature	40° – 110° F (4° – 43° C)
Operating Humidity	20% – 80% non-condensing
Storage Temperature	0° – 125° F (-18° – 57° C)
Storage Humidity	5% – 95% non-condensing

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The LPS11-S is shipped ready to operate in one of three configurations:

a. Standard box with slide guides installed for rack mounting.

b. Tabletop model with "super cover."

c. As part of a DEC computer system.

Figure 2-1 illustrates the packaging used for shipping the LPS11-S. If the equipment is to be rack-mounted, necessary hardware is shipped with the unit. The LPS11-S does not require any special shipping mounts.

2.2 UNPACKING

CAUTION

Do not attempt to unpack, install, or interface the LPS11-S until DEC has been notified and a Field Service Representative is present; otherwise, the warranty may be voided.

To unpack the LPS11-S, carefully remove the unit and all accessories from the shipping container. Conduct an inventory to ensure that all of the required items are included.

After removing the unit from the shipping container, inspect it for damage. It is advisable to save the packing carton, in case it should become necessary to return the unit for service.

2.3 MECHANICAL DESCRIPTION

Figure 1-1 shows the LPS11-S mounting box (5-1/4 in. by 19 in. by 20 in.) with super cover. The removable top cover of the mounting box is fastened by four cam-lock screws. The removable side panel is fastened by four Phillips-head screws.

Figure 2-2 shows the LPS11-S mounting box with the top cover removed. The backplane unit divides the power supply from the side of the mounting box containing the bus control and options.

Figure 2-3 shows the mounting box with the top cover and side panel removed, and the bus control and option modules plugged in. This is a fully-expanded LPS11-S.

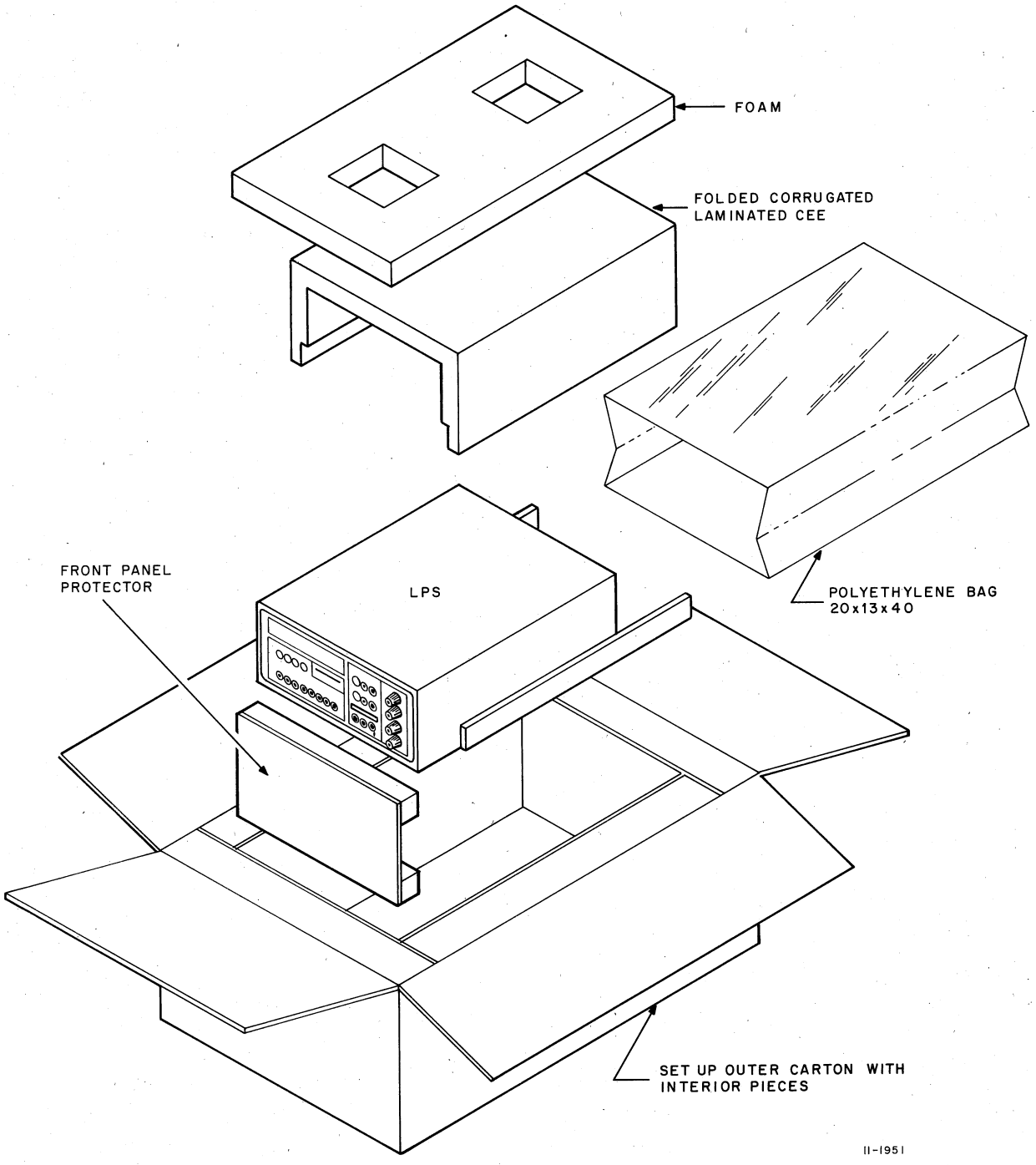

Figure 2-1 LPS11-S Packaging

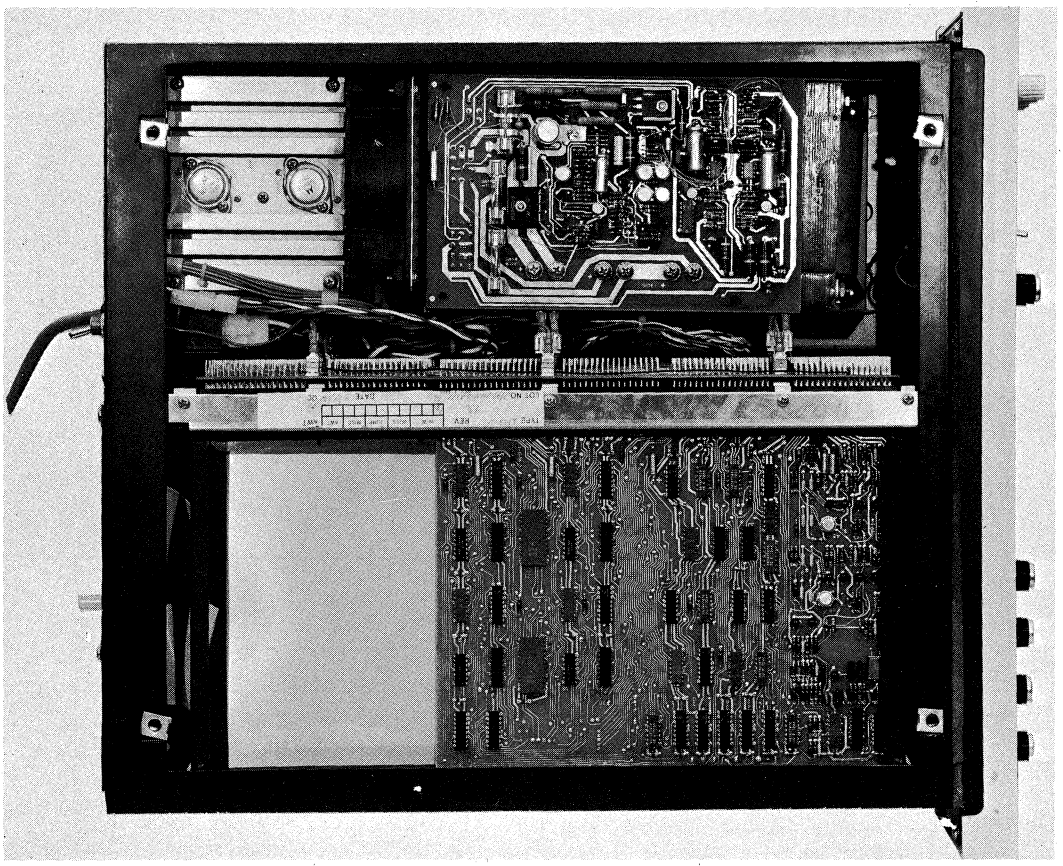

Figure 2-2 LPS11-S with Top Cover Removed

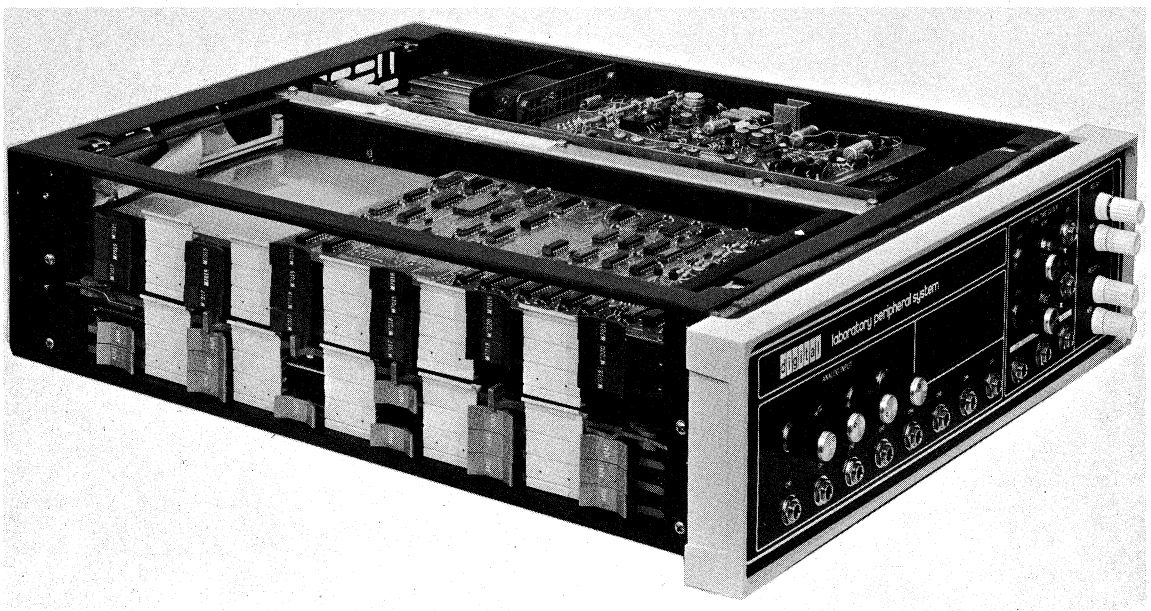

Figure 2-3 LPS11-S Mounting Box with Top Cover and Side Panel Removed

Figure 2-4 shows the mounting box complete with modules, together with a guide illustrating the option slot allocations. Module guides assist in inserting the modules into the proper slots.

Figure 2-5 is a rear view of the mounting box. An ON/OFF power switch is provided for maintenance purposes. The power control circuit breaker protects the power supply from overload.

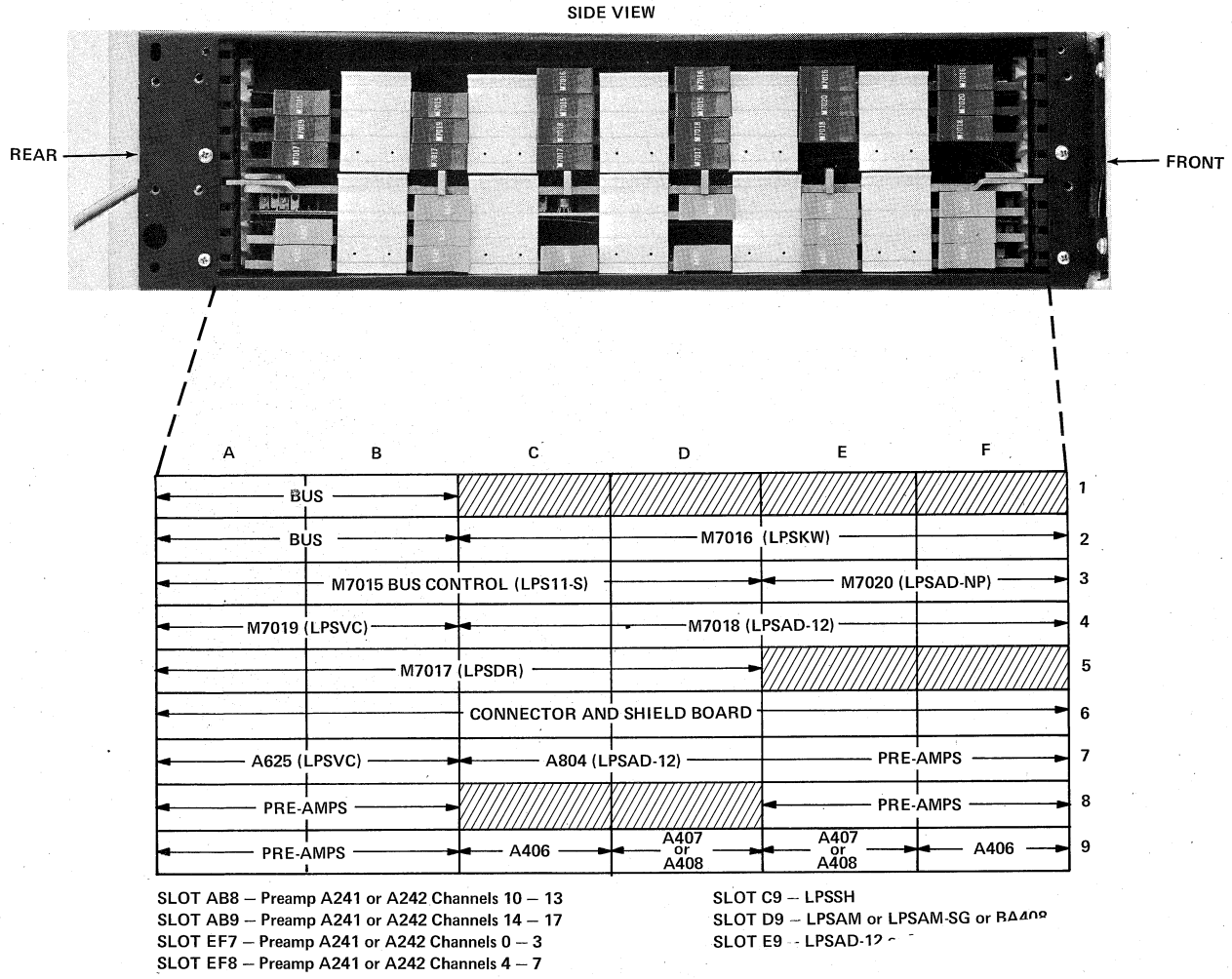

Figure 2-4 LPS11-S Option Slot Allocations

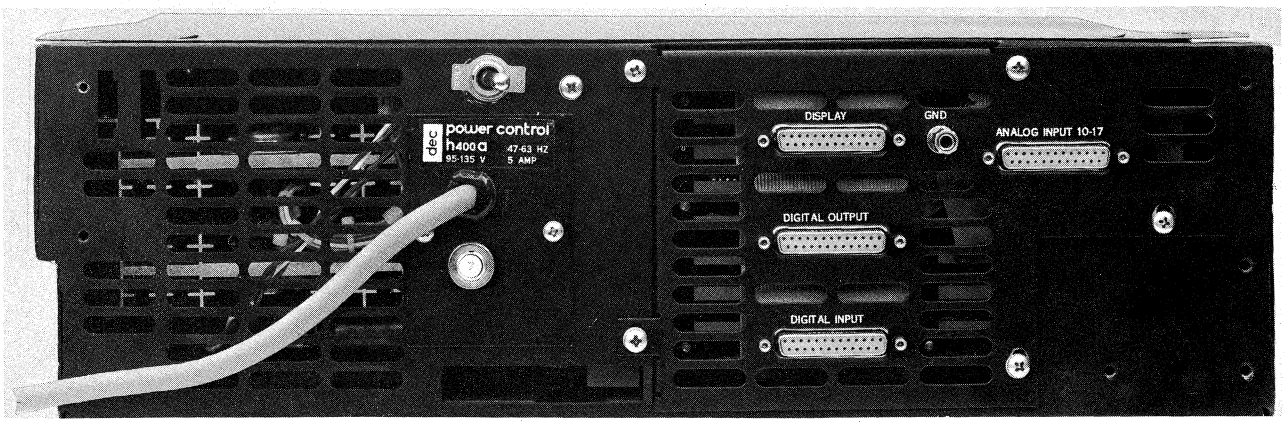

Figure 2-5 LPS11-S Rear View

2.4 INSPECTION

Prior to operating the equipment, conduct a complete visual examination of all external controls, indicators, cables, and connectors, as well as all internal components that could have become loosened or damaged as a result of shipping and handling.

After it has been established that the equipment is not physically damaged, conduct a continuity check of the power supply of the LPS11-S. Using an ohmmeter, ensure that no short circuits exist between the following backplane pins:

a. Pins A01-A2 (+5V supply) and A01-C2 (Ground)

b. Pins A09-D2 (+15V supply) and A09-F2 (Ground)

c. Pin A09-D2 and any A09-C2 pin

d. Pins A09-D2 and A09-E2 (−15V supply)

e. Pin A09-E2 and any A09-C2.

2.5 AC POWER REQUIREMENTS

The LPS11-S is capable of operating from either a 115 or 230V, 50 or 60 Hz power source, depending upon the installation of the power supply power control. Figure 2-5 shows the location of the power control unit. Power input connections are shown on drawing D-UA-LPS11-S-0, sheet 3. The associated circuit breaker requirements are listed in Table 2-1.

Table 2-1
115/230V Jumper and Circuit Breaker Configuration

Line Voltage	Option	Jumper	Circuit Breaker
115	SA, SC, SD, SF	BC05H	7 Amperes
230	SB, SF	BC05J	4 Amperes

If the prime power source of the LPS11-S is not provided by the host computer system, it is recommended that a line be provided separate from those containing power for the lighting, air conditioning, or other general equipment so that the system will not be affected by fluctuations in line voltage. If the system is to be installed in an electrically noisy environment, it may be necessary to condition the ac power line or to provide a suitable earth ground. The DEC Field Service Representative can assist in determining whether the environment is suitable for the LPS11-S.

Before plugging in the unit, measure the outlet receptacle voltage level with an ac voltmeter to ascertain the power source voltage level.

CAUTION

To protect against electrical shocks, ensure that the LPS11-S and case are properly grounded before applying power to the unit. If the equipment is installed outside the United States or where the national electric code does not govern building wiring, extreme caution should be exercised.

If the ground integrity is questionable, it is advisable to measure the potential difference between the case and a known ground with an ac voltmeter.

2.6 INITIAL TURN-ON

When energizing the LPS11-S for the first time and prior to interfacing the system with the host computer, turn on the unit according to the instructions in the following paragraphs. If any of the indicators should prove other than normal, calibrate the unit according to the instructions in Chapter 4.

CAUTION

Do not attempt to operate the LPS11-S until the continuity check described in Paragraph 2.4 has been completed satisfactorily.

1. Insert the ac line cord plug into the appropriate power receptacle (Paragraph 2.5).

2. Ensure that the ON/OFF maintenance power switch on the rear of the LPS11-S is set to the ON position.

3. Use a dc voltmeter to ensure that voltages at the backplane pins specified in Table 2-2 are within the specified tolerances.

Table 2-2
LPS11-S Power Checks

Positive Lead	Negative Lead	Voltage
Pin A01-A2	Pin A01-C2	+5 Vdc
Pin A09-D2	Pin A09-F2	+15 Vdc
Pin A09-F2	Pin A09-E2	-15 Vdc

4. Using an oscilloscope, check the voltages listed in Table 2-2 to ensure that they do not exceed a 1% tolerance.

If the voltages are correct, set the ON/OFF switch to OFF, disconnect the line cord, and interface the LPS11-S with the host computer as described in Paragraph 2.7.

2.7 SYSTEM INSTALLATION

The LPS11-S Laboratory Peripheral System mounts in a standard 19-in. wide by 20-in. deep equipment bay. The unit is mounted on slides for easy access. To mount the unit, first attach the fixed portion of the slides to the cabinet. (The fixed portion of the slides can be removed from the LPS11-S by actuating the slide release.) The slides should be mounted so that the fixed guides are parallel to and level with the ground.

When the slide guides have been securely fastened to the cabinet, using all eight screws, lift the unit and slide it carefully onto the slide guides until the slide release locks. Lift the slide release gently and push the unit fully into the rack, taking care not to tear any existing cabling.

Extend the unit fully until the slide release locks. If the installation of cables is required, remove the top cover of the LPS11-S. The cover is removed by loosening and removing four cam-lock screws.

2.8 CABLE INSTALLATION

The LPS11-S is shipped with all internal cables installed. Check that all cables are properly mated before interfacing the unit with the host computer.

The Unibus cable is installed in the following manner:

1. Remove the top cover and side panels from the LPS11-S.
2. Loosen the captive screws securing the rear connector panels.
3. Insert the cable through the slot at the top of the rear connector panels.
4. Insert the cable connector in the appropriate slot (A2/B2 as shown in Figure 2-4).
5. Insert the bus terminator in slot A1/B1.

2.9 OPTION INSTALLATION

The system is shipped with all of the purchased options installed. The following paragraphs describe the manner in which options are installed into an existing system in case of expansion at a later date.

2.9.1 LPSAD-12 A/D Converter

The LPSAD-12 A/D Converter is installed in the following manner:

1. Remove the top cover and side panel from the LPS11-S mounting box.
2. Remove the bus control module (M7015) from the unit. (See Figure 2-4 for location in slots A3/B3/C3/D3.)
3. Remove split-lug jumper A from the bus control module and reinsert the bus control module into slots A3/B3/C3/D3.
4. Insert the A/D module (M7018) into slots C4/D4/E4/F4.
5. Insert the A/D converter module (A804) into slots C7/D7.
6. Check that the only channel-select jumper installed on multiplexer module A407 is the one that corresponds to channels 0–7.
7. Insert the multiplexer module (A407) into slot E9.
8. Insert the sample-and-hold module (A406) into slot F9.
9. Insert the extender modules on the left handles of both jumper cards.
10. Insert one of the jumper cards into slots E7/F7. Insert the other jumper card into slots E8/F8.
11. Replace the top cover and side panel on the LPS11-S.
12. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSAD-12 A/D Converter option is installed properly and operating correctly.

2.9.2 LPSAD-NP Direct Memory Access (DMA)

The LPSAD-NP Direct Memory Access option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.
2. Remove the grant continuity card from slot E3 (Figure 2-4).
3. Insert the DMA module (M7020) into slot E3/F3.
4. Replace the top cover and side panel of the LPS11-S.
5. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSAD-NP option is installed properly and operating correctly.

2.9.3 LPSAM 10–17 Channel Multiplexer

The LPSAM 10–17 Channel Multiplexer option is installed in the following manner:

1. Check that only the 10–17 channel select jumper is installed on the multiplexer module (A407).
2. Check that the 0–7 ONLY jumper has been removed from the multiplexer module.
3. Insert the multiplexer module into slot D9 (Figure 2-4).
4. Insert the extender modules on the right side of the jumper modules.
5. Insert one of the jumper modules into slot A8/B8 and the other into slot A9/B9.
6. Remove the screws securing the rear connector panel to the mounting box, and open the panel as far as cable lead length will allow.
7. Remove modules as required to permit access to the connector panel. Attach the cable assembly (using the hardware supplied) to the ANALOG INPUT 10–17 slot.
8. Route the cable through the card guide assembly between slots 5 and 6 and insert the connector into the A/D module connector on the M996.
9. Replace all of the modules removed in step 7.
10. Replace the rear connector panel and secure the Unibus cable as described in Paragraph 2.8.
11. Replace the top cover and side panel of the LPS11-S.
12. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSAM 10–17 Channel Multiplexer option is installed properly and operating correctly.

2.9.4 LPSAG Preamplifier

The LPSAG Preamplifier option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.
2. Remove the G728 card from the four-channel slot in which the option is to be installed.

Slot E7/F7 = Channels 0–3
Slot E8/F8 = Channels 4–7
Slot A8/B8 = Channels 10–13
Slot A9/B9 = Channels 14–17

3. Replace the G728 with the LPSAG (A242) module.

4. Replace the top cover and side panel of the LPS11-S.

2.9.5 LPSAG-VG Preamplifier

The LPSAG-VG Preamplifier option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.

2. Remove the G728 card from the four-channel slot in which the option is to be installed.

   Slot E7/F7 = Channels 0–3
   Slot E8/F8 = Channels 4–7
   Slot A8/B8 = Channels 10–13
   Slot A9/B9 = Channels 14–17

3. Place the plug-in jumpers in the correct input range position for each of the four channels.

4. Replace the G728 with the LPSAG-VG (A241) module.

5. Replace the top cover and side panel of the LPS11-S.

2.9.6 LPSSH Dual Sample-and-Hold

The LPSSH Dual Sample-and-Hold option is installed in the following manner:

NOTE
Installation of the dual sample-and-hold module presupposes that the A/D converter and channels 0–17 have been installed.

1. Remove the top cover and side panel from the LPS11-S.

2. Insert the sample-and-hold module (A406) into slot C9 (Figure 2-4).

3. Remove the multiplexer (A407) from slot E9 and remove jumper W1 from the module.

4. Insert the multiplexer into slot E9.

5. Replace the top cover and side panel of the LPS11-S.

6. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures to ensure that the LPSSH Dual Sample-and-Hold option is installed properly and operating correctly.

2.9.7 LPSKW Real-Time Clock

The LPSKW Real-Time Clock option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.

2. Remove the bus control module (M7015) from the LPS11-S.

3. Remove the jumper designated B from the bus control module, and reinsert the module into slots A3/B3/C3/D3 (Figure 2-4).

4. Insert the clock module (M7016) into slots C2/D2/E2/F2.

5. Replace the top cover and side panel of the LPS11-S.

6. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSKW Real-Time Clock option is installed properly and operating correctly.

2.9.8 LPSVC Display Control

The LPSVC Display Control option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.

2. Remove the bus control module (M7015) from slots A3/B3/C3/D3 of LPS11-S (Figure 2-4).

3. Remove the jumper marked E from the bus control module, and reinsert the module into the LPS11-S.

4. Check that the appropriate jumper arrangements on the scope control module (M7019) and the D/A converter module (A625) are correct for the type of scope to be employed with the system.

5. Remove the screws securing the rear connector panel and open the panel as far as cable lead lengths will allow.

6. Remove modules as required to permit access to the connector panel.

7. Attach the scope control cable to the DISPLAY slot.

8. Route cables through card guide assembly between slots 5 and 6.

9. Connect the cable to the DISPLAY connector on the M996 module.

10. Replace the modules removed in step 6.

11. Insert the scope control module (M7019) into slots A4/B4.

12. Insert the D/A converter module (A625) into slots A7/B7.

13. Install the top cover and side panel of the LPS11-S.

14. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSVC Display Control option is installed properly and operating correctly.

2.9.9 LPSDR Digital Input/Output

The LPSDR Digital Input/Output option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.

2. Remove the bus control module (M7015) from the LPS11-S.

3. Remove jumpers C and D from the bus control module.

4. Insert the bus control module (M7015) into slots A3/B3/C3/D3 (Figure 2-4).

5. Insert the digital I/O module (M7017) into slots A5/B5/C5/D5.

6. Remove the screws securing the rear connector panel and open the panel as far as cable lead length will allow.

7. Remove modules as required to permit access to the connector panel.

8. Attach the longer of the two cable connectors (using the hardware supplied) to the DIGITAL OUTPUT slot. Connect the shorter cable connector to the DIGITAL INPUT slot.

9. Route both cables through card guide assembly between slots 5 and 6.

10. Connect the cables to their respective input and output connectors designated D I/O INPUT and D I/O OUTPUT, respectively, on the M996 module.

11. Replace the modules removed in step 7.

12. Replace the rear connector panel and secure the Unibus cable.

13. Insert the two identical relays into the relay sockets located on the inside of the front panel. Attach the relay retaining clips to secure the relays in place.

14. Replace the top cover and side panel of the LPS11-S.

15. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSDR Digital Input/Output option is installed properly and operating correctly.

2.9.10 BA408 Switched Gain Multiplexer (Channels 0–7)

The BA408 Switched Gain Multiplexer option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.

2. Remove the H755 power supply from the LPS11-S.

3. Remove the A407 Fixed Gain Multiplexer module from slot E09.

4. Install ECOs on A/D Control Board M7018 and backpanel as described in the *LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure* (A-SP-LPSAM-SG-2).

5. Check that W2 is in the "0–7" position on the A408 module.

6. Insert the A408 module into slot E09.

7. Install the magnetic shield in the H755 as shown in the H755 print set (E-UA-H755-0-0).

8. Replace the H755 in the LPS11-S.

9. Conduct an acceptance test as described in the LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure to ensure that the BA408 Switched Gain Multiplexer option is installed properly and operating correctly.

10. Install the top cover and side panel of the LPS11-S.

2.9.11 LPSAM-SG Switched Gain Multiplexer (Channels 10–17)

The LPSAM-SG Switched Gain Multiplexer option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.
2. Ensure that a BA408 option has already been installed in channels 0–7 per Paragraph 2.9.10. (Switched gain and fixed gain multiplexers may not be mixed.)
3. Check that W2 is in the "10–17" position on the A408 Switched Gain Multiplexer.
4. Insert the Switched Gain Multiplexer module into slot D09 (Figure 2-4).
5. Attach the extender handles to the end of the G728 jumper modules.
6. Insert one of the jumper modules into slot A8/B8 and the other into slot A9/B9.
7. Remove the screws securing the rear connector panel to the mounting box; open the panel as far as the cable lead length will allow.
8. Remove modules as required to permit access to the connector panel. Attach the cable assembly (using the hardware supplied) to the ANALOG INPUT 10–17 slot.
9. Route the cable through the card guide assembly between slots 5 and 6 and insert the connector into the A/D 10–17 connector on the M996 Connector Shield Board.
10. Replace all of the modules removed in step 7.
11. Replace the rear connector panel and secure the Unibus cable as described in Paragraph 2.8.
12. Conduct an acceptance test as described in the LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure (A-SP-LPSAM-SG-2) to ensure that the LPSAM-SG 10–17 Switched Gain Multiplexer channels 10–17 option is installed properly and operating correctly.
13. Replace the top cover and side panel of the LPS11-S.

2.9.12 BA408 Switched Gain Multiplexer (Channels 10–17)

The BA408 Switched Gain Multiplexer option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.
2. Remove the fixed gain MUX A407 from slot D09.
3. Ensure that a BA408 option has already been installed in channels 0–7 per Paragraph 2.9.10. (Switched gain and fixed gain multiplexers may not be mixed.)
4. Check that W2 is in the "10–17" position on the A408 module.
5. Insert the A408 module into slot D09.
6. Conduct an acceptance test as described in the LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure, to ensure that the BA408 Switched Gain Multiplexer option is installed properly and operating correctly.
7. Install the top cover and side panel of the LPS11-S.

CHAPTER 3
THEORY OF OPERATION

3.1 BUS CONTROL

The Unibus interface module (bus control) consists of three functional sections: address control, internal bus, and interrupt and priority logic. Figure 3-1 contains a block diagram of the bus control, which is discussed below.

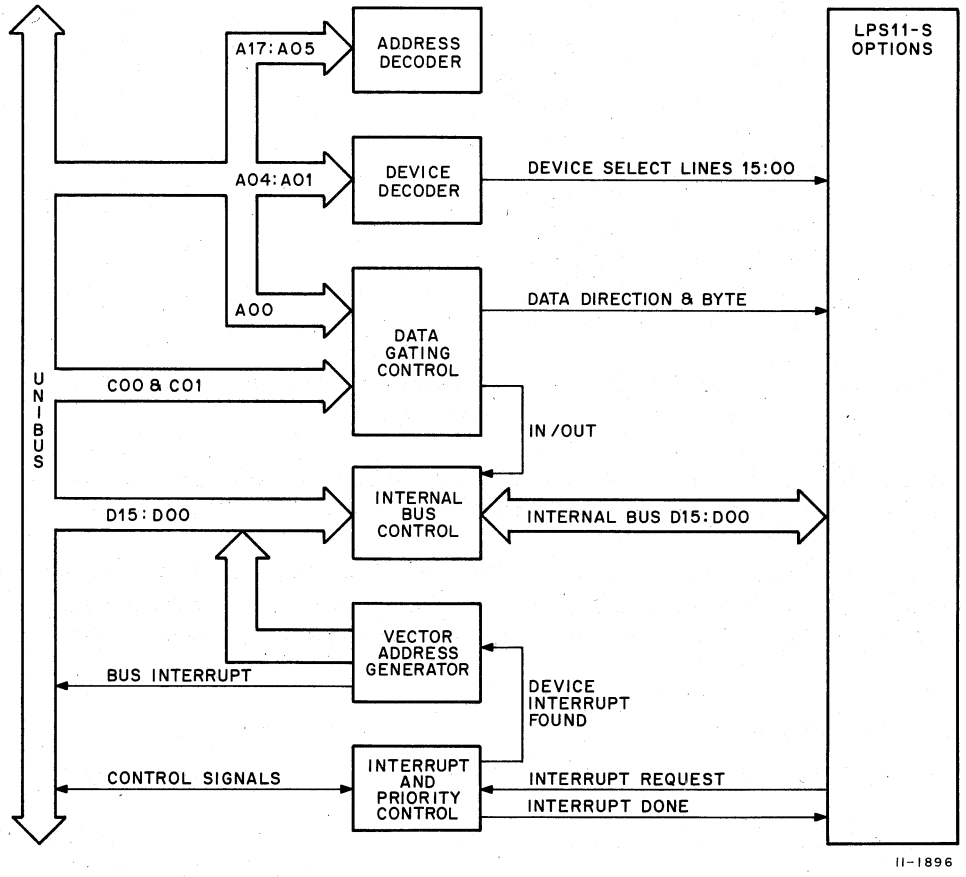

Figure 3-1 Bus Control Block Diagram

3.1.1 Block Diagram Discussion

The address control section enables the addressing of the option registers of the LPS11-S. When the unit is addressed, the address control decodes the Unibus address lines A17:A05, and allows Unibus address lines A04:A01 to be loaded into a 4-to-16 decoder. The decoder interrogates Unibus A04:A01, and sends a select signal to the device that is addressed.

Table 3-1 lists the LPS11-S option register address assignments.

Table 3-1
LPS11-S Option Address Assignments

Address	Option Register Assignments
770400	A/D Status Register
770402	A/D Buffer (read) and LED (write) Registers
770404	Clock Status Register
770406	Clock Buffer Register
770410	D I/O Status Register
770412	D I/O Input Register
770414	D I/O Output Register
770416	D/A Status Register
770420	D/A X Register
770422	D/A Y Register
770424	Ext DAC
770426	Expansion
770430	Expansion
770432	Expansion
770434	Expansion
770436	Direct Memory Access Registers

When the addressed LPS11-S option is installed, it initiates the signals required to request control of the bus. After the bus request is granted, the bus performs the function indicated.

The internal bus logic drives and receives external Unibus data and internal data. The address control supplies the internal bus logic with data direction and byte control by decoding Unibus A00, C00, and C01 signals.

The interrupt and priority logic determines which option issued the interrupt request and services the highest assigned priority interrupt request first. At the completion of the interrupt, the control automatically returns and checks for any more requests. Each of the interrupt request lines has an associated floating vector address in memory.

3.1.2 LPS11-S Option Addressing

Eighteen address lines are used to address the LPS11-S. The address register bit assignments are shown in Figure 3-2.

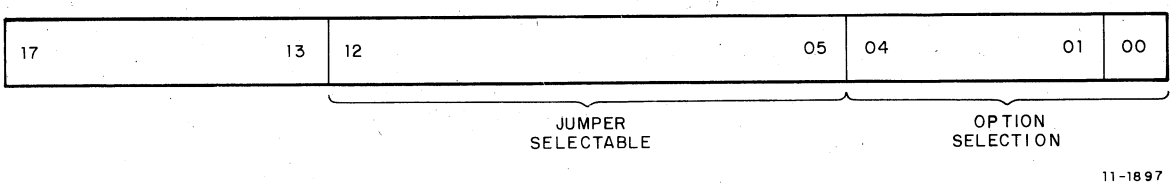

Figure 3-2 Address Register Bit Assignments

The LPS11-S is factory-configured for the option addresses specified in Table 3-1. However, a floating block address enables the user to locate the block of 16 addresses anywhere from address 600000 to 777740 by jumpers A12–A5. If the jumper arrangements are altered, the respective order will remain the same.

NOTE

If jumpers A12–A5 are changed, special care must be taken that the new addresses do not conflict with any existing address on the PDP-11 Unibus.

3.1.3 Address Control

The address control logic accepts any block of 16 consecutive addresses (Table 3-1) where the starting address is defined by the selection of split lug jumpers A12–A5. Figure 3-3 shows the operation of the address control logic.

When the correct address appears on Unibus A17:A05 and BUS MSYN (Bus Master Synchronization) is received, ENABLE is generated to indicate that the LPS11-S has been addressed.

Unibus A04:A01 are strobed into the 4–16 option decoder by the ENABLE signal, enabling one of 16 LPS11-S option SELECT lines, as defined in Table 3-2. The option responds to the SELECT line by producing the signal I BUS ENABLE RT, which is a hard-wire ORed internal bus signal generated by each option.

Table 3-2
4–16 Option Decoder

Bus A Lines				Select Signal	Option	Device Code	Control Module
04	03	02	01				
0	0	0	0	0	ADSR	A	M7018
0	0	0	1	1	ADBR	A	M7018
0	0	1	0	2	CKSR	B	M7016
0	0	1	1	3	CKBR	B	M7016
0	1	0	0	4	D I/O SR	C	M7017
0	1	0	1	5	D I/O IN	C	M7017
0	1	1	0	6	D I/O OUT	D	M7017
0	1	1	1	7	D/A SR	E	M7019
1	0	0	0	8	D/A XR	E	M7019
1	0	0	1	9	D/A YR	E	M7019
1	0	1	0	10	EXT DAC	E	M7019
1	0	1	1	11	EXPANSION	F	
1	1	0	0	12	EXPANSION	F	
1	1	0	1	13	EXPANSION	F	
1	1	1	0	14	EXPANSION	F	
1	1	1	1	15	DMA	A	M7020

Signal I BUS ENABLE RT is delayed 100 ns to become BUS SSYN and is returned to the bus master to acknowledge device or register selection. If a SELECT line is enabled and the option selected is not installed, I BUS ENABLE RT is not generated. Therefore, BUS SSYN will not be generated and the CPU will time out and trap.

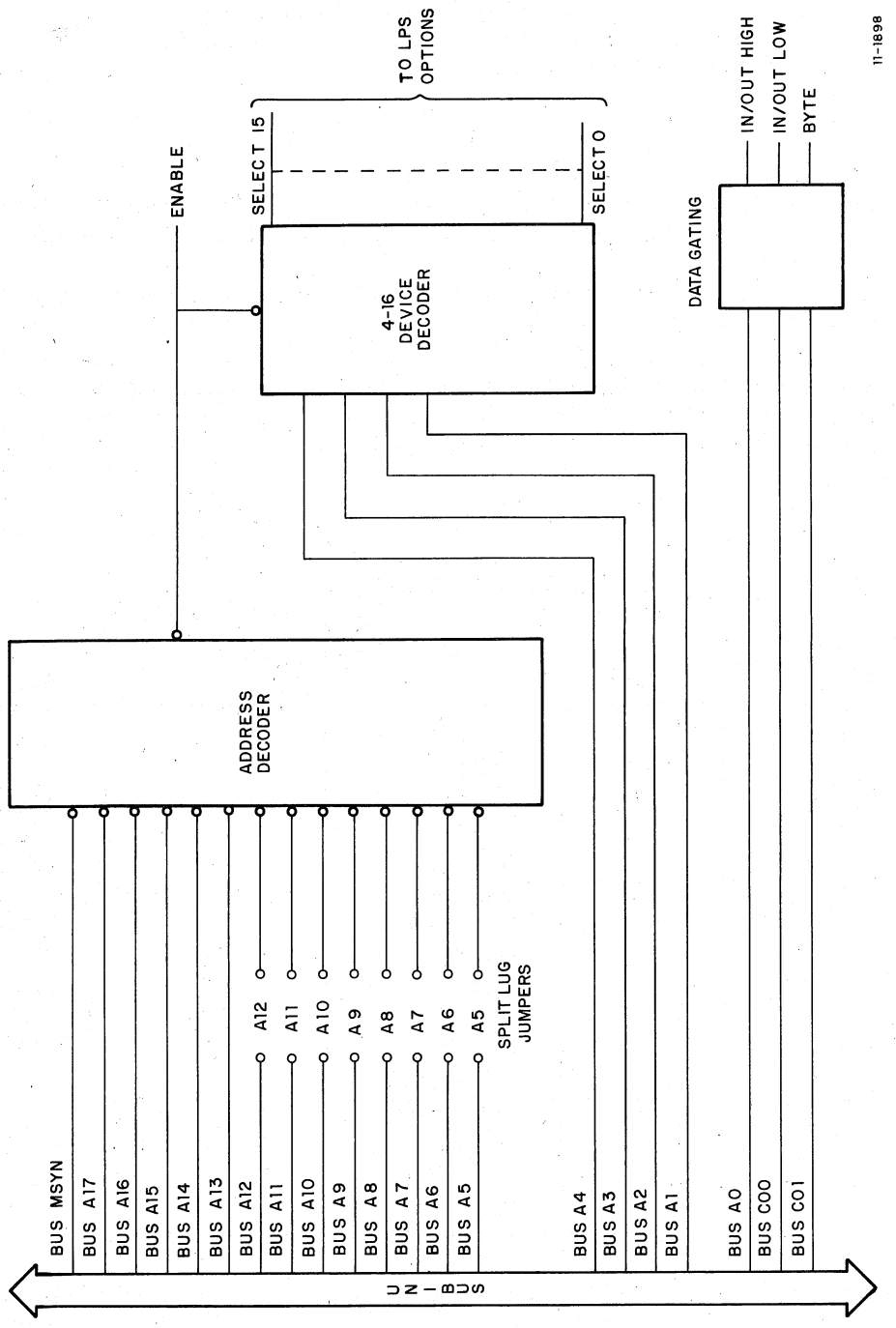

Figure 3-3 Address Control Logic

3.1.4 Internal Bus

The LPS11-S internal bus is a buffer between the Unibus and the bus used by the LPS11-S options, providing one unit load on the Unibus.

When the direction of data is out (from the processor to the LPS11-S), Unibus D15:D00 are gated to the internal bus by OUT HIGH and OUT LOW signals, as shown in Table 3-3.

Table 3-3
Data Transfer

Unibus Signals			LPS11-S Signal Names	Transfer Explanation
C00	C01	A00		
H	H	N/A	IN	Gates the LPS11-S internal bus onto the Unibus.
L	H	N/A	IN	Gates the LPS11-S internal bus onto the Unibus.
H	L	N/A	OUT HIGH OUT LOW	Gates a full 16-bit word from the Unibus onto the LPS11-S internal bus.
L	L	L	OUT HIGH	Gates D15:D08 of the Unibus onto the internal bus.
L	L	H	OUT LOW	Gates D07:D00 of the Unibus onto the internal bus.

When the direction of data is in (from the LPS11-S to the processor), I BUS D15:D00 from the internal bus are gated onto the Unibus by the signal IN. Figure 3-4 shows the operation of the internal bus logic.

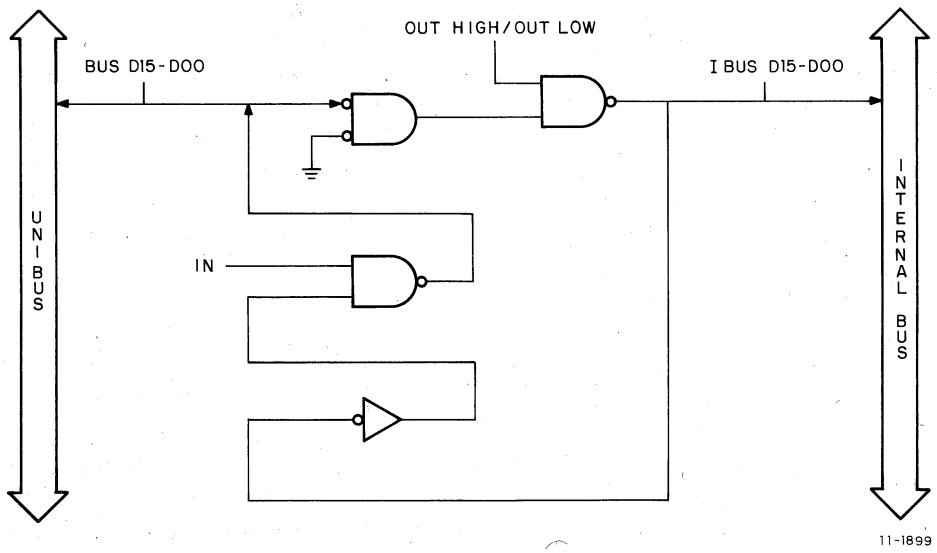

Figure 3-4 Internal Bus Logic

3.1.5 Interrupt and Priority Logic

NOTE
The discussion herein assumes that the reader is familiar with the interrupt concept of the PDP-11.

The LPS11-S interrupt scheme utilizes six interrupts, each at a selectable bus priority. The six priority levels are factory-set to the configuration specified in Table 3-4. The priority levels can be changed where necessary by jumper sockets A–F, as shown in Figure 3-5.

Table 3-4
Standard Priority Configuration

Option Designation	Internal LPS11-S Option Codes	Bus Priority
LPSAD	INT A	6
LPSKW	INT B	5
LPSDR	INT C	4
LPSDR	INT D	4
LPSVC	INT E	4
Undefined	INT F	4

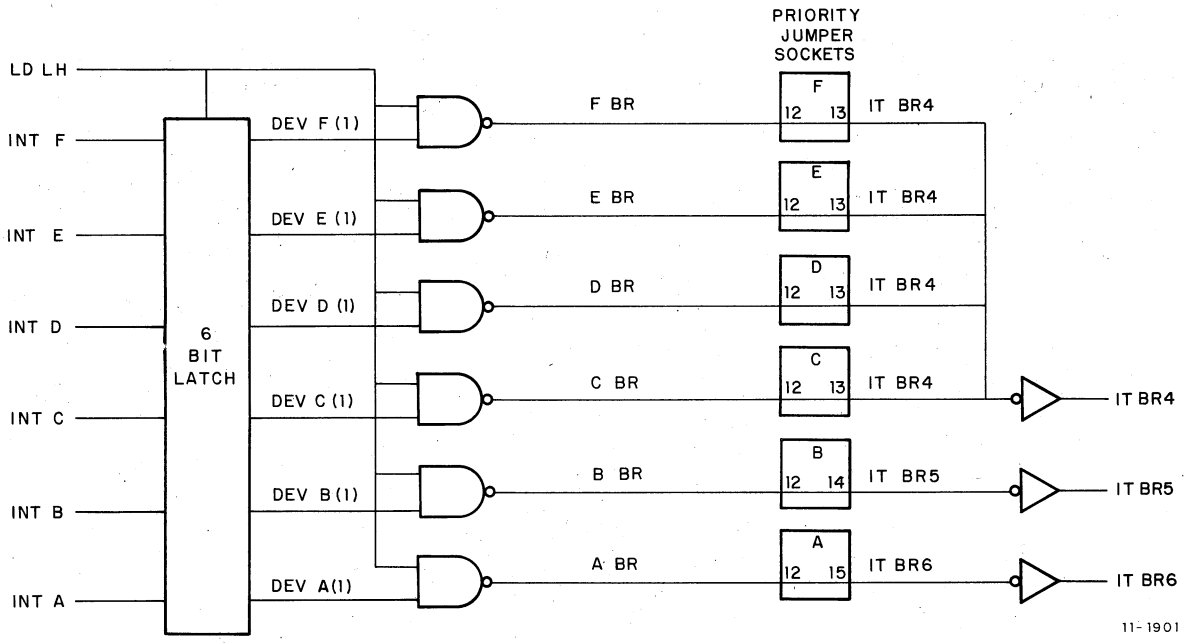

Figure 3-5 Bus Request Logic

If the standard priority configuration shown in Table 3-4 is employed, an interrupt could be initiated by the LPSVC scope control option, for example, by generating INT E. When INT E is generated and the bus control is not processing an interrupt, END (0), the direct clear side of flip-flop FF1, goes high, enabling the clock input. INT E is clocked by LD LH (Load Latch) into a 6-bit latch circuit (Figure 3-6), which is used by the interrupt control to identify the device issuing the interrupt.

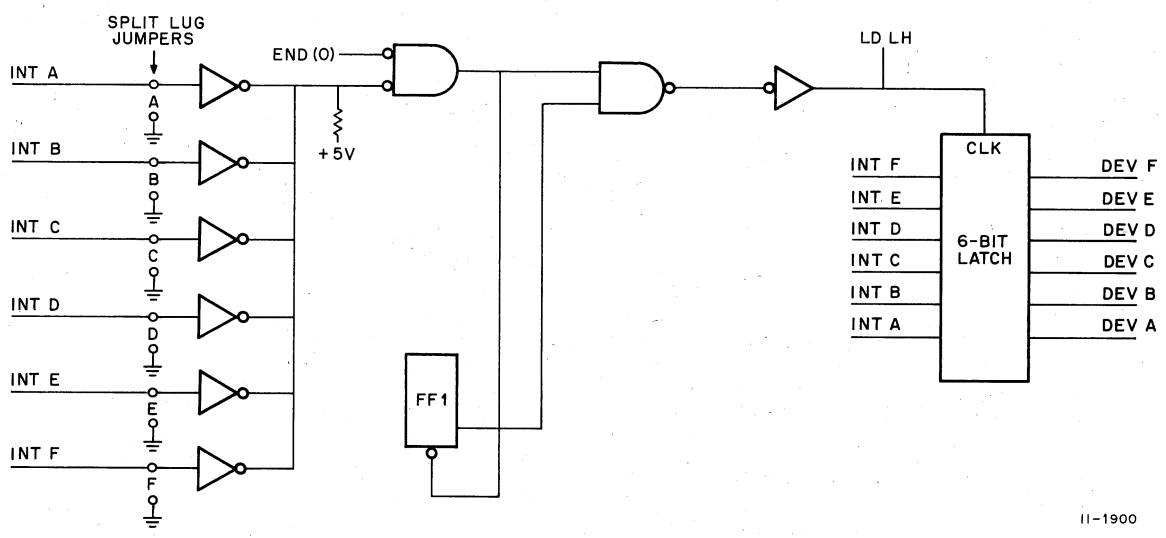

Figure 3-6 6-Bit Latch Logic

LD LH also gates bus request E BR on the bus request line through priority jumper socket E, where it becomes signal IT BR 4 to the PDP-11 priority arbitration circuit, as shown in Figure 3-5.

NOTE

Devices C, D, E, and F are all tied together on the Bus Request 4 line. If all four devices simultaneously created interrupts and were latched up in the 6-bit latch, device C would be granted the bus because it is physically closest to the processor.

If the bus request can be granted, the processor returns a bus grant in (BUS BG4 IN) signal (Figure 3-7). Because priority jumper and socket (PJS) A and B are not on bus grant level 4, the BUS BG4 signal is passed through PJS A and B, and is applied to PJS C. The priority jumper installed in socket C inhibits the level from being passed further and the signal becomes BGC IN (Figure 3-8). BGC IN is buffered and generates the signal BGC, which triggers a 100 ns delay, during which BGC is ANDed with DEV C (0) (an output of the 6-bit latch) to interrogate whether device C initiated the bus request. Because device C did not, the FF1 flip-flop is not set and, after 100 ns, the MUX generates BGC OUT.

BGC OUT is then routed through PJS C and passed onto PJS D to become BGD IN, and the process described above is repeated to produce BGD OUT, which is routed through PJS D to PJS E. At PJS E, BGD OUT becomes BGE IN.

Bus grant level BGE IN is buffered to create BGE, and the 100 ns delay is triggered once again. Because device E (DEV E) did create the bus request, the FF1 flip-flop sets during the 100 ns delay, inhibiting the MUX from passing the bus request along to PJS F. Setting of FF1 also generates LD INT to latch the device being granted the bus into INT HOLD LATCH, whose output is EE (1), and creates BUS SACK (Bus Acknowledge), which indicates to the processor that the device that created the bus request has been identified. When the processor receivers BUS SACK, BUS BG4 is disqualified and is ANDed with GR ENABLE to set the FF2 flip-flop.

Setting of FF1 and FF2 enables the interrupt vector address to be gated onto BUS D08:D02 lines (Figure 3-9). The interrupt vector address is the sum of the initial starting address, specified by the D08:D02 jumper arrangement, and the device offset. Table 3-5 shows standard vector address assignments.

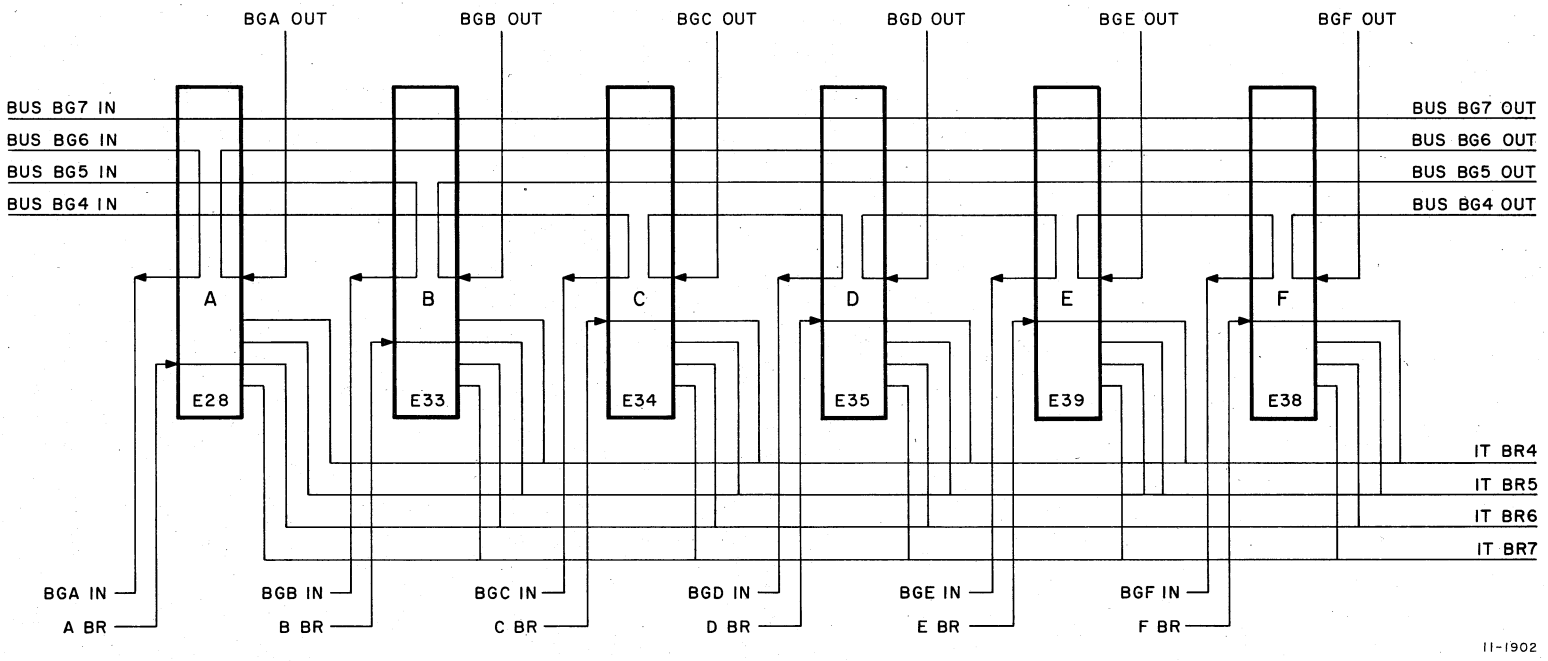

Figure 3-7 Standard Priority Jumper Configuration

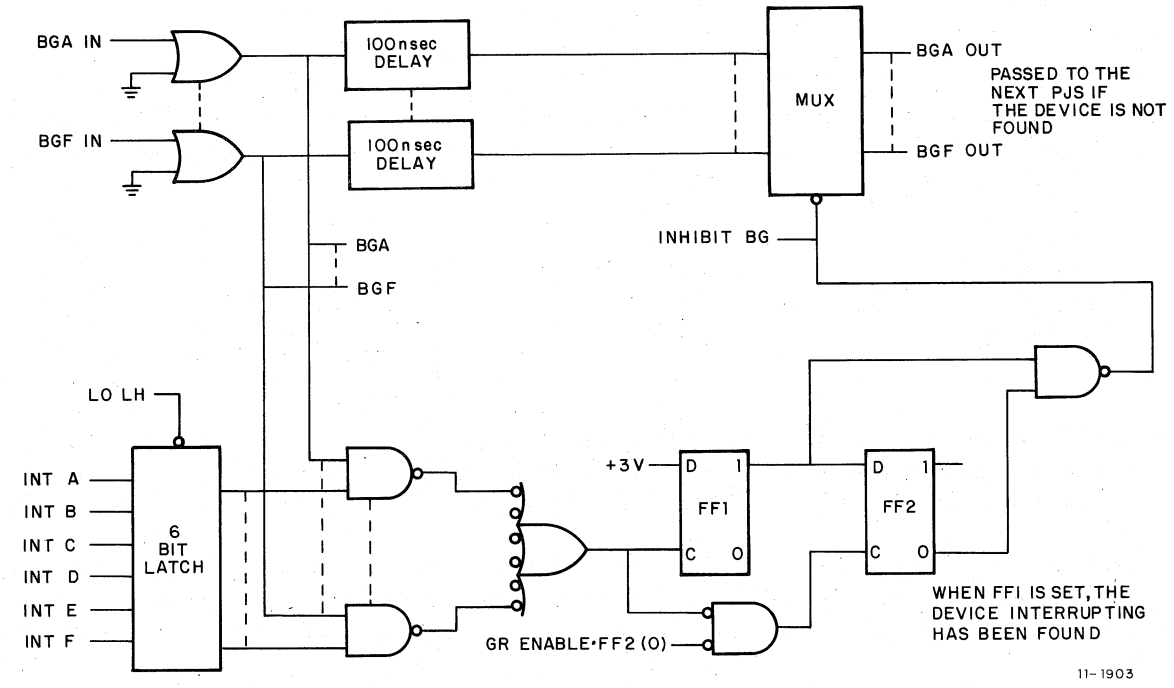

Figure 3-8 Bus Grant Inhibit Logic

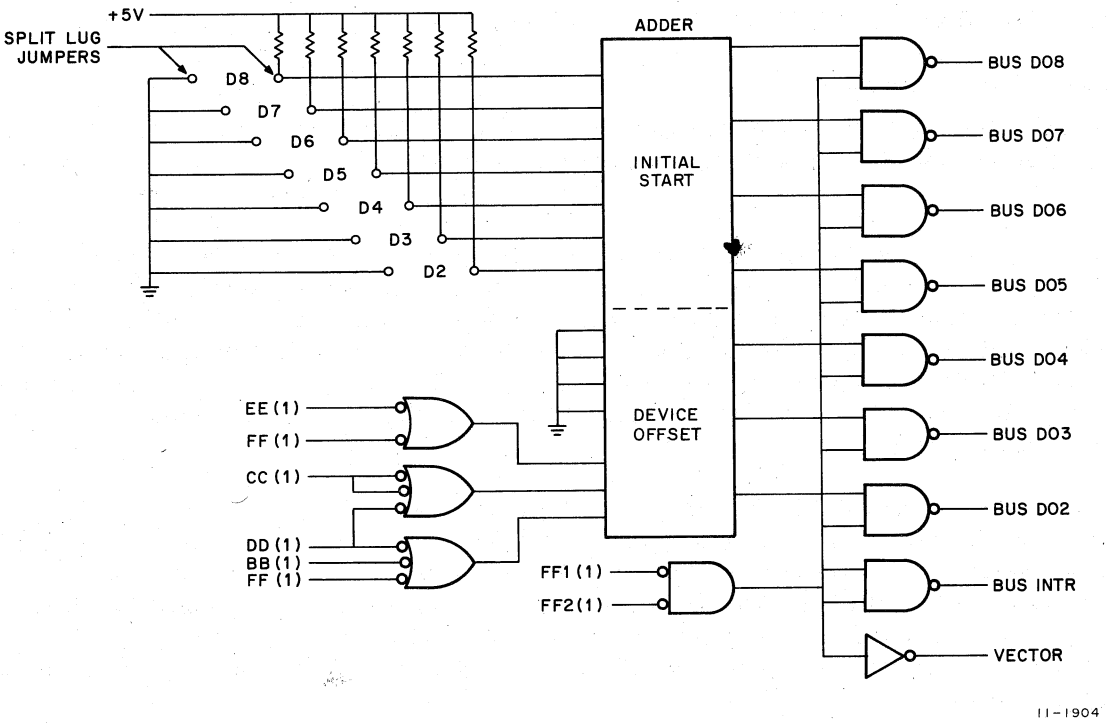

Figure 3-9 Vector Address Adder

Table 3-5
Standard Vector Address Assignments

Option Designation	Internal LPS11-S Option Codes	Bus Priority	Vector Address
LPSAD	INT A	6	300
LPSKW	INT B	5	304
LPSDR	INT C	4	310
LPSDR	INT D	4	314
LPSVC	INT E	4	320
Undefined	INT F	4	324

Setting FF2 also asserts BUS BBSY, which in effect tells the processor that all conditions have been met, and that a device is taking control of the bus. The assertion of BUS BBSY disqualifies GR ENABLE, disabling other devices on the bus from taking control. The BUS INTR signal tells the processor to start a program interrupt (Figure 3-10).

The processor responds with BUS SSYN, which is ANDed with the signal VECTOR to direct set the END flip-flop and clear the 6-bit latch that held the initial device interrupt request. The END flip-flop also generates INT DONE E, telling device E that the interrupt is completed. Device E then removes INT REQ E and clears the FF1 and FF2 flip-flops.

Clearing FF1 and FF2 removes BUS BBSY. The processor removes BUS SSYN to clear the END flip-flop, which, in turn, triggers a 100 ns delay and clears the INT HOLD LATCH, leaving the bus control ready to process the next interrupt.

3.2 ANALOG-TO-DIGITAL CONVERTER SYSTEM

3.2.1 Block Diagram Discussion

The basic LPS11-S analog-to-digital system (Figure 3-11) consists of an A/D control and an analog section. The A/D control module comprises four logic sections: Status register, LED and A/D buffer, A/D control logic, and interrupt control.

The Status register is used to control the operation of the LPSAD-12 and LPSAD-NP options by starting conversions, enabling interrupts, selecting channels, etc. The LED register and A/D buffer share a single read/write address, which is used for the two different functions. The write-only address controls a 6-digit numeric front panel display that includes a sign and decimal point, and the read-only address contains the converted A/D value. The A/D control logic provides the necessary control and error logic to ensure proper operation and relationship of the LPSAD-12 to the associated options. The interrupt control provides the required control signals to the Unibus control to initiate bus requests.

The analog section of the LPSAD-12 consists of a 12-bit A/D converter, sample-and-hold, and an 8-channel multiplexer. The first 8 channels (0–7) of the analog subsystem are connected to phone jack inputs on the front panel, permitting direct interfacing with laboratory equipment. The first 4 channels (0–3) can be adapted to either internal or external signals. Each is connected to a front panel potentiometer, which can establish parameters, set thresholds, etc. The insertion of phone plugs into the jacks disables the output voltage of the associated potentiometers, making it possible to apply external analog input either directly to the multiplexer or to an optional 4-channel preamplifier.

When an A/D conversion is initiated, the analog input from a selected channel is gated by the 8-channel multiplexer to the single sample-and-hold circuit, where it is held until it is digitized by the A/D converter by the successive approximation technique of conversion. The resultant output is then transferred to the A/D buffer as a right-justified, offset binary number.

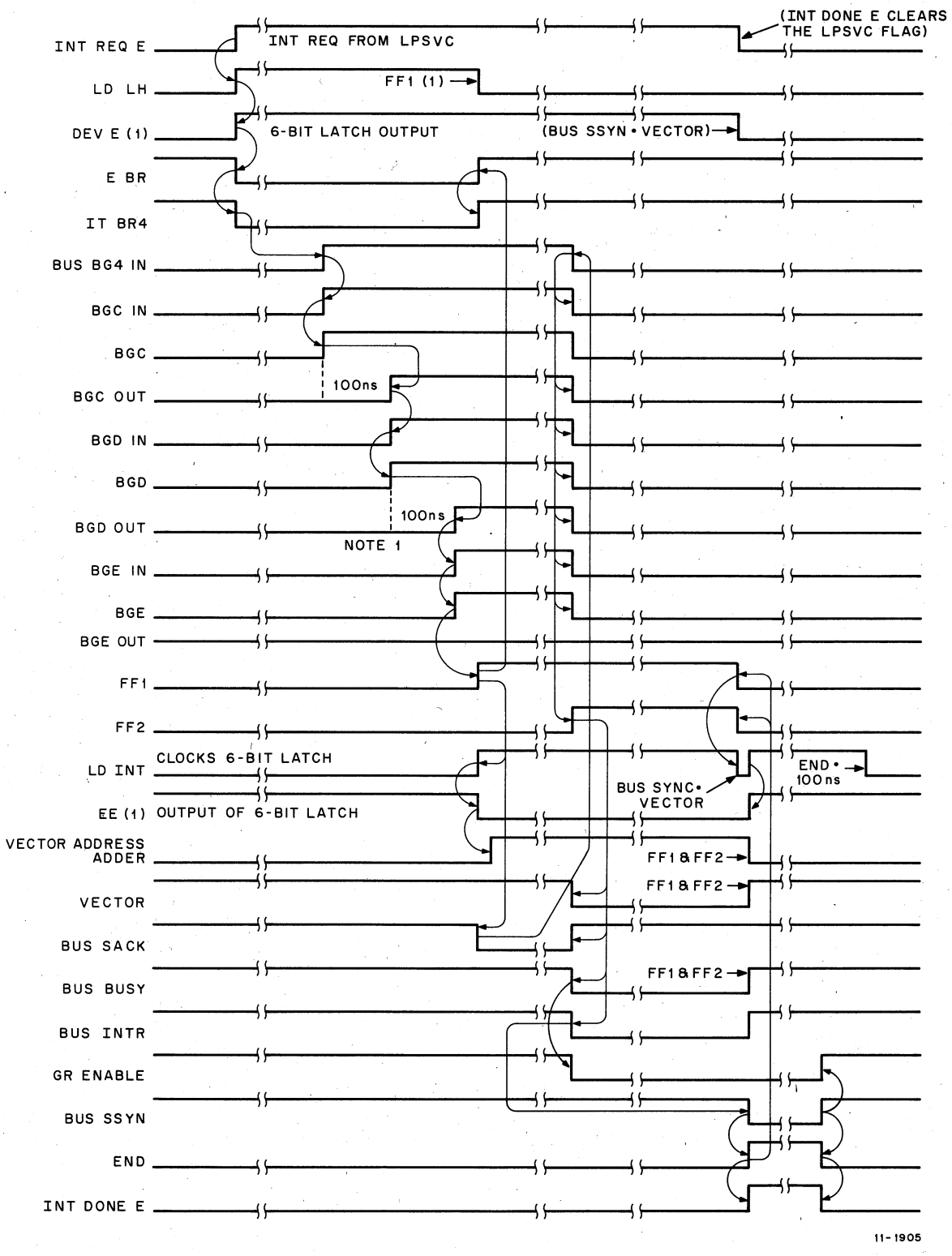

Figure 3-10 Interrupt Timing

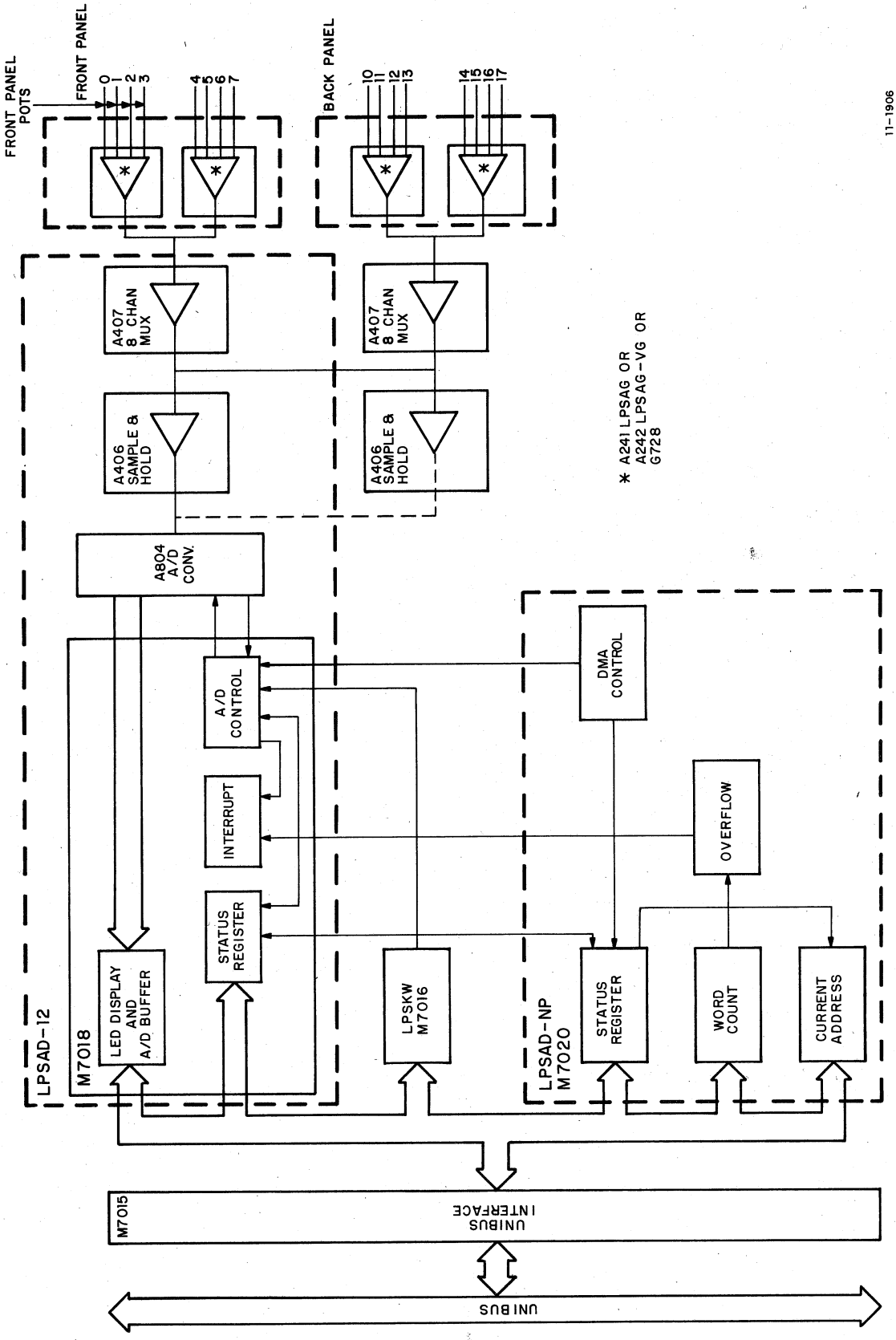

Figure 3-11 A/D Converter Block Diagram

The analog system may be expanded to include fixed- or variable-gain preamplifiers and an additional 8-channel multiplexer, giving an available total of 16 channels. The added 8 channels (10–17) are accessible via the back panel of the LPS11-S. An optional second sample-and-hold circuit may be added to facilitate special analog data acquisition requirements, making it possible to sample two channels simultaneously. The resultant analog values can be converted into two 12-bit values sampled at precisely the same time.

The LPSAD-12 A/D subsystem may also be used in conjunction with the LPSAD-NP direct memory access option or the LPSKW real-time clock option. The LPSAD-NP, which transfers converted analog data to memory at a maximum rate without program intervention, consists of a Status register, word count, and a current address with associated control and timing circuit.

The Status register contains the extended address bits, error bit, and DMA enable bit. The Word Count register contains the 2's complement of the number of words transferred. At the completion of the transfer, the DMA interrupts the processor by a word count overflow. The Current Address register contains the starting address where transfers are stored.

The real-time clock (LPSKW) can be used to initiate A/D conversions either at a predetermined rate or based on an external event via the Schmitt trigger.

3.2.2 A/D Programming

The analog subsystem of the LPS11-S utilizes two registers, the A/D Status register and the A/D buffer and LED register.

3.2.2.1 A/D Status Register – The Status register is illustrated in Figure 3-12, and defined in Table 3-6. In addition to the theory of operation detailed in this chapter, additional programming information regarding the Status register and its functions may be found in the *LPS11-S User's Guide.*

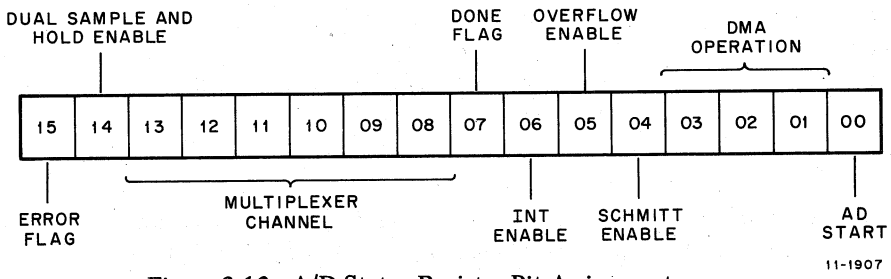

Figure 3-12 A/D Status Register Bit Assignments

Table 3-6
A/D Status Register Bit Functions

Bit	Name	Meaning and Operation
15	ERROR flag (Read only)	This bit is set when: a. A second A/D start is initiated before the first conversion is complete. b. A second A/D conversion ends before data from the previous conversion is read. c. The multiplexer is changed during the first μsecond of an A/D conversion. This bit is cleared when loaded or upon INIT.

Table 3-6 (Cont)
A/D Status Register Bit Functions

Bit	Name	Function
14	Dual Mode Enable (Read/Write)	1 = Dual Sample-and-Hold Mode 0 = Single Sample-and-Hold Mode
13–08	Mux Channel (Read/Write)	Defines which analog channel is to be sampled.
07	DONE flag (Read only)	Set upon conversion of an A/D conversion. Cleared by hardware when an interrupt is completed or when the A/D buffer register is read.
06	Interrupt Enable (Read/Write)	When a conversion is completed, the DONE flag will cause an interrupt if this bit = 1.
05	Overflow Enable (Read/Write)	If the LPSKW real-time clock is part of the system, a clock overflow initiates a conversion if this bit = 1.
04	Schmitt Enable (Read/Write)	If the LPSKW real-time clock is part of the system, enabling this bit permits an external event to initiate an A/D conversion via Schmitt trigger #1.
03–01	DMA Register Bits (Read/Write)	These bits are used in conjunction with the LPSAD-NP option. For normal operation the bits are 0. (Refer to Paragraph 3.2.11, Direct Memory Access.)
00	A/D Start (Read/Write)	Setting this bit initiates an A/D conversion. It is cleared at the end of the conversion.

3.2.2.2 LED and A/D Buffer Register – When used as a read-only register (Figure 3-13), this register contains the right-justified, offset binary 12-bit conversion of the last analog conversion (Table 3-7).

Table 3-7
A/D Converter Digital Output With No Offset Applied

Analog Input Voltage	12-Bit Result
Maximum + Voltage	007777
Minimum + Voltage	004001
Zero Volts	004000
Minimum - Voltage	003777
Maximum - Voltage	000000

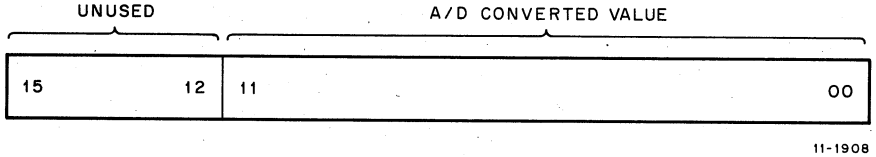

Figure 3-13 A/D Buffer Bit Assignments as a Read-Only Address

When used as a write-only register (Figure 3-14), this register programs the LED display on the front panel, selecting the appropriate LED and digit, as defined in Table 3-8.

Table 3-8
LED Register Bit Functions

Bits	Bit Function
15–11	Not used
10–08	Defines LED Address:

Bits	10	09	08	LED
	0	0	0	LED 1 (LSD)
	0	0	1	LED 2
	0	1	0	LED 3
	0	1	1	LED 4
	1	0	0	LED 5
	1	0	1	LED 6
	1	1	0	Unused
	1	1	1	Unused

07–05	Not used
04	When set, illuminates decimal point in addition to numeral.
03–00	Selects numeral to be displayed:

Bits	03	02	01	00	Numeral Displayed
	0	0	0	0	= 0
	0	0	0	1	= 1
	0	0	1	0	= 2
	0	0	1	1	= 3
	0	1	0	0	= 4
	0	1	0	1	= 5
	0	1	1	0	= 6
	0	1	1	1	= 7
	1	0	0	0	= 8
	1	0	0	1	= 9
	1	0	1	0	= Test pattern
	1	0	1	1	= Blank
	1	1	0	0	= Blank
	1	1	0	1	= - (minus)
	1	1	1	0	= Blank
	1	1	1	1	= Blank

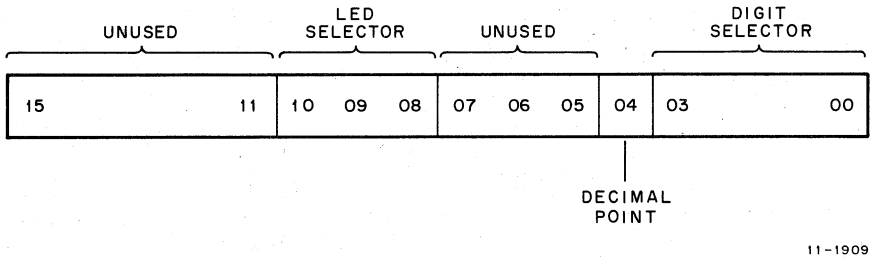

Figure 3-14 LED Register Bit Assignments as a Write-Only Address

3.2.3 Error Flag

There are several error conditions that can set the A/D Error flag (bit 15 of the Status register). One of these is met if the 8-channel multiplexer is changed during the first μsecond after the switch from sample to hold. This condition is checked by the 1 μs HOLD DELAY signal ANDed with MC DLY (multiplexer channel delay), which is caused by loading the upper byte of the A/D Status register, to direct set the ERR flip-flop (Figure 3-15).

A second error condition exists when an A/D request is issued while conversion is still in process (ST00 or EOCP). The third error condition exists when the previously converted A/D value in the A/D buffer has not been read (SAVE flip-flop still set) and a second end-of-conversion pulse (EOCP) occurs.

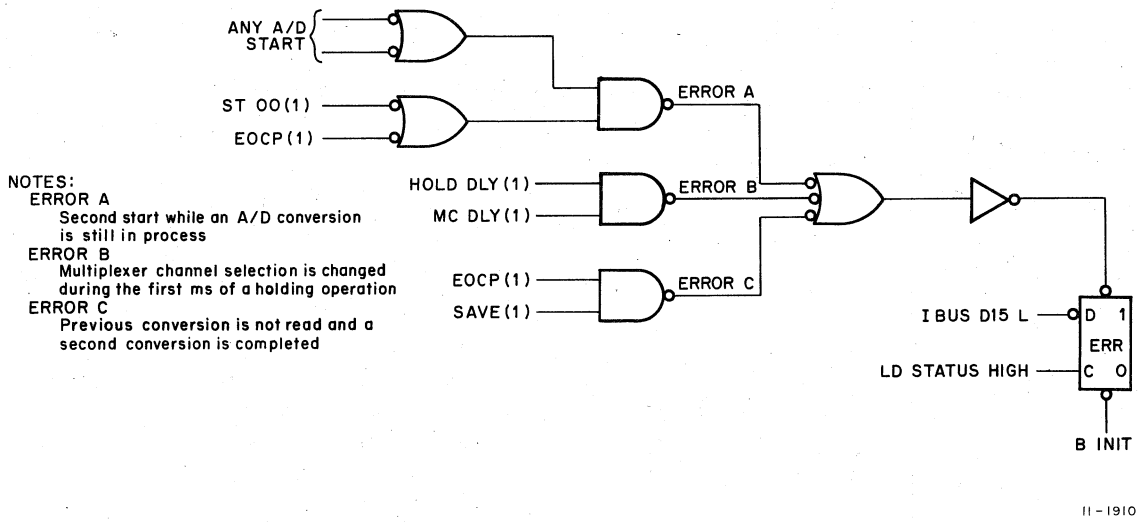

Figure 3-15 A/D Error Detection Logic

3.2.4 Addressing

A/D addressing covers the manner in which the various registers are addressed, as well as the signals involved. The bus control decodes Unibus lines A17:A01 and enables one of two select lines, 0 and 1, to the A/D control when addressed. (Paragraph 3.1 contains a detailed discussion of the bus control operation.) The two select lines are ANDed with the IN/OUT signals to become the read and write commands (Figure 3-16).

SELECT 0 is used to address the Status register to enable read/write functions, including byte operations, to be performed. SELECT 1 ANDed with IN addresses the A/D buffer (read only); SELECT 1 ANDed with OUT addresses the LED register (write only).

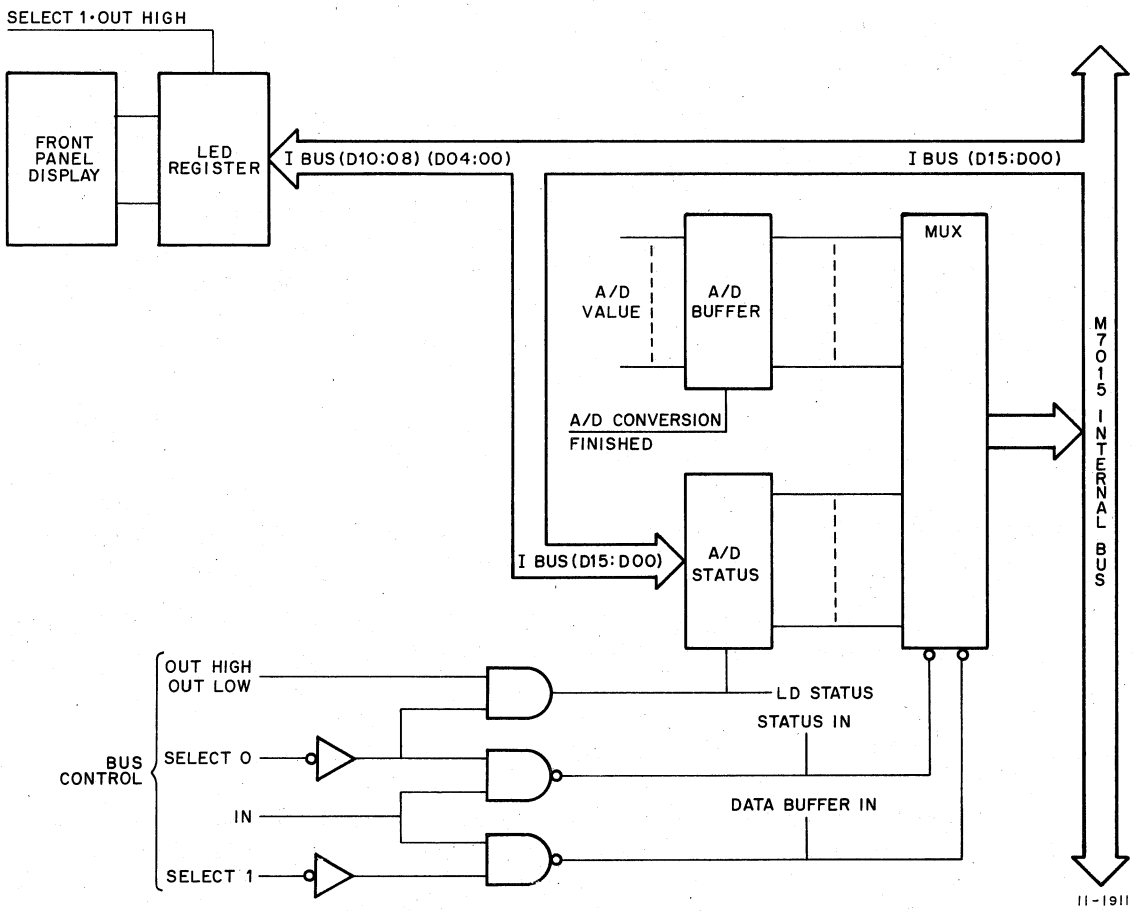

Figure 3-16 A/D Addressing Logic

The select 0 and 1 lines are also used to create the I BUS ENABLE RT signal, which is returned to the Unibus to acknowledge that the A/D control has been selected.

3.2.5 LED Buffer

When SELECT 1 is used as a write-only input, it becomes the LED display address. Bits 8, 9, and 10 decode which of the individual LEDs is being loaded. These bits are applied to a decoder where six ENA signals are generated. SELECT 1 and OUT trigger a one-shot multivibrator, and the output is used to enable the decoder. The data (bits 0–4) is buffered and applied to all six numeric displays. The ENA signal loads the selected LED with data, causing it to light.

3.2.6 A/D Conversion Starts

A/D conversions can be initiated by program starts, clock overflows, or Schmitt trigger firings.

3.2.6.1 Program Starts – For program starts, the Status register is loaded with control bits (refer to Paragraph 3.2.3, A/D Programming) and bit 0 = 1. The LD STATUS LOW (Figure 3-17) is ANDed with I BUS D00 to trigger the PST (Program Start) one-shot multivibrator. The PST acts as a delay to allow the 8-channel multiplexer time to settle out.

At the end of PST delay, the HOLD flip-flop is set, triggering the HOLD DELAY one-shot multivibrator and permitting the sample-and-hold circuits to settle in HOLD mode. At the end of the HOLD DELAY, the ST00 flip-flop is set, enabling the A/D converter to perform the conversion on the hold sample.

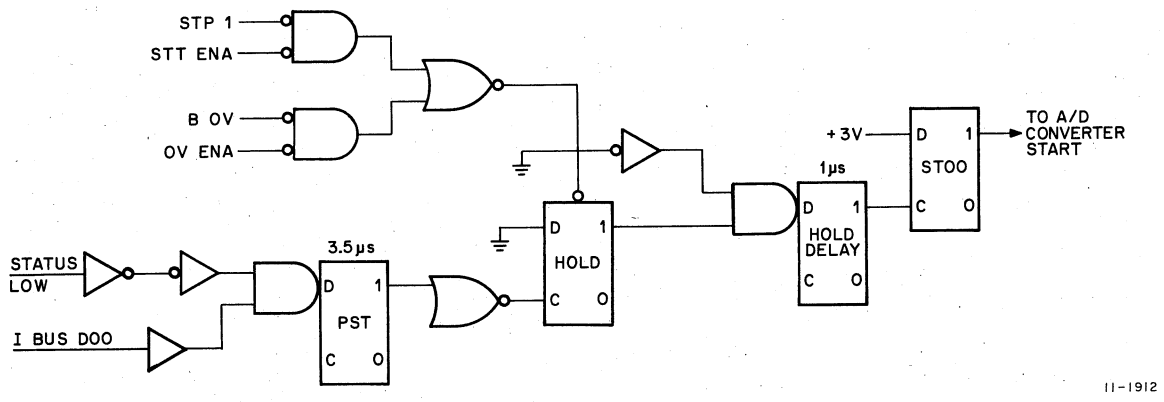

Figure 3-17 Program and Clock A/D Start Logic

3.2.6.2 Clock Overflow – If the LPSKW option is installed and bit 5 of the A/D Status register is set (clock overflow enable), an overflow of the LPSKW clock counter initiates an A/D conversion (Figure 3-17).

The clock overflow signal, B OV, is ANDed with OV ENA (bit 5 of Status register) to set the HOLD flip-flop, which, in turn, triggers the HOLD DELAY one-shot multivibrator, permitting the sample-and-hold circuits to settle in HOLD mode.

At the end of the HOLD DELAY, the ST00 flip-flop is set, enabling the A/D converter to start a conversion.

3.2.6.3 Schmitt Trigger #1 – If the LPSKW option is installed and bit 4 of the A/D Status register is set (Schmitt trigger enable), an external event can initiate an A/D conversion via Schmitt trigger #1 (Figure 3-17).

The Schmitt trigger #1 signal, STP 1, is ANDed with STT ENA (bit 4 of the A/D register) to set the HOLD flip-flop, which triggers the HOLD DELAY one-shot multivibrator, permitting the sample-and-hold circuits to settle in HOLD mode.

At the end of the HOLD DELAY, the ST00 flip-flop is set, enabling the A/D converter to start a conversion.

3.2.7 A/D Conversion Timing

The setting of the ST00 flip-flop enables the A/D converter to perform one conversion. The conversion time of the A/D converter depends on the word length selected: 12-bit = 19 µs, 10-bit = 8 µs, 8-bit = 4.5 µs. The conversion time is determined by setting the word length selector switch on the A/D converter module (A804) to the appropriate position and adjusting the A/D clock (via R23 on A804) for the required time.

At the completion of the conversion, the A/D converter returns the end-of-conversion (EOC) signal, triggering the EOCP one-shot multivibrator (Figure 3-18). When in the basic LPSAD-12 configuration, the EOCP clears the ST00, HOLD, and HOLD SAVE flip-flops and sets the SAVE and DONE flip-flops.

3.2.8 Interrupt

If the interrupt is enabled by INT ENA (bit 6 of the A/D Status register) and the DMA is not enabled (DMA), setting the DONE flip-blop (bit 7 of Status register) initiates an interrupt request (INT REQ A) (Figure 3-18). When the bus control processes the interrupt, INT DONE A is returned to the A/D control, clearing the DONE flip-flop.

If the interrupt is not enabled, the software must check the Status register for the DONE flag. When the A/D buffer is read, the DATA BUFFER IN signal clears the SAVE and DONE flip-flops. If the A/D buffer is not read, the SAVE flip-flop remains set. If the A/D buffer is not read before the next conversion, an error condition will result.

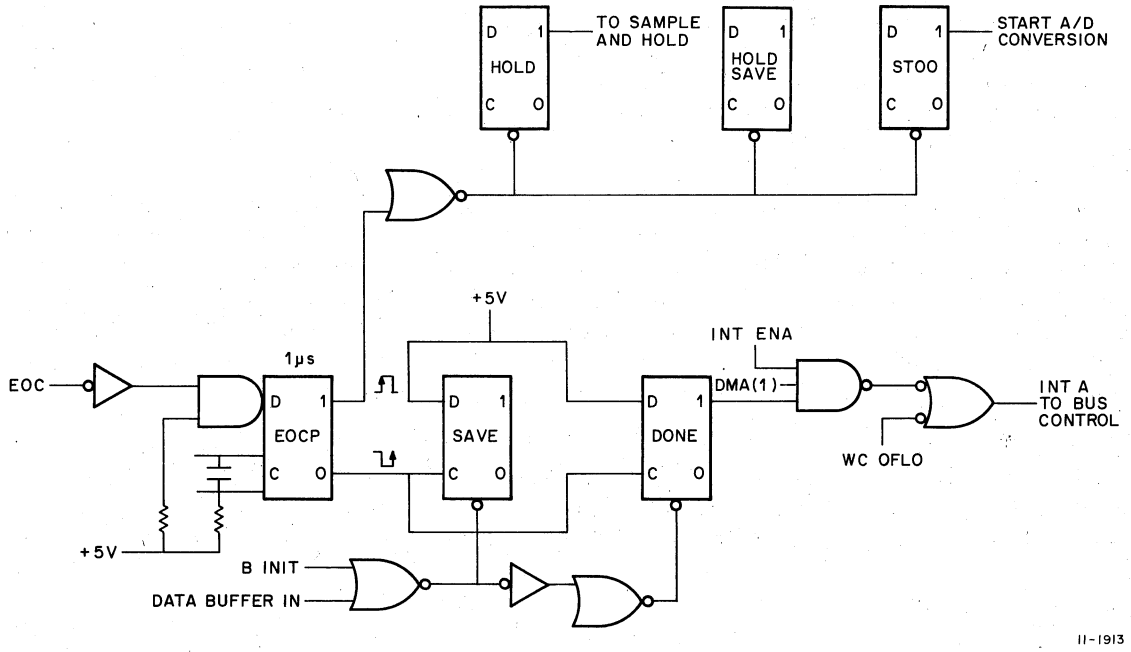

Figure 3-18 Basic EOCP Functions and Interrupt Logic

3.2.9 Dual Sample-and-Hold

The dual sample-and-hold option (LPSSH) makes it possible to hold two simultaneous samples from two different analog channels. The dual sample-and-hold module, when installed, returns a ground (DUAL MODE) to the A/D control (Figure 3-19). When set, DUAL ENA (bit 14 of the Status register) is ANDed with DUAL MODE to enable the dual operation.

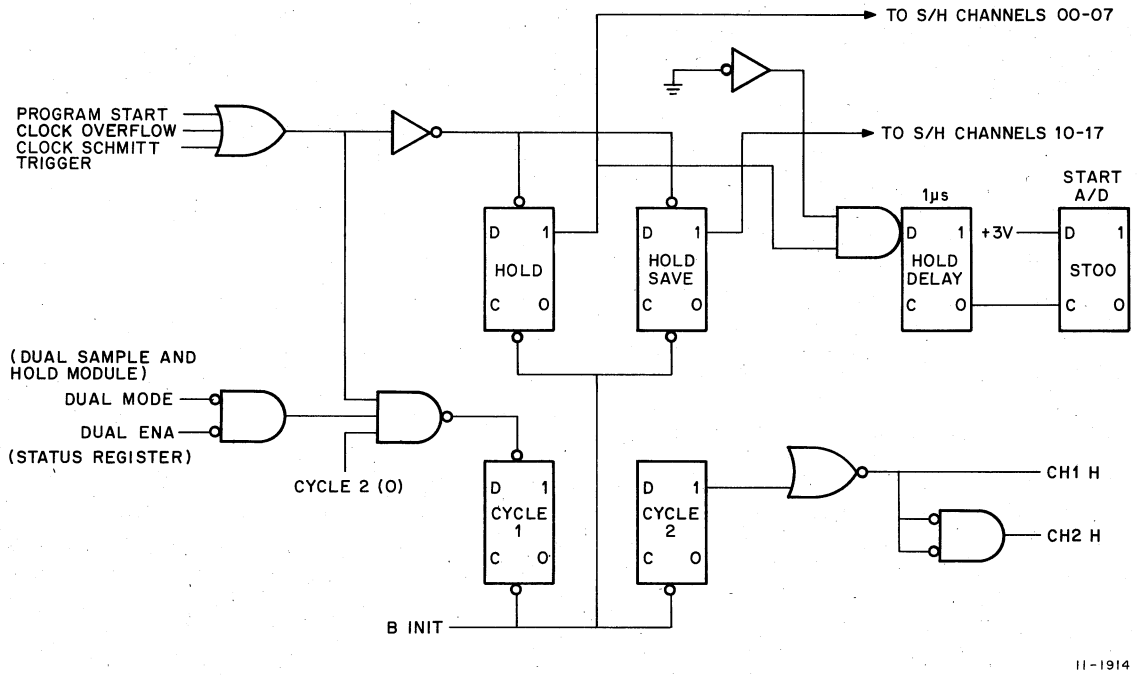

Figure 3-19 Dual Sample-and-Hold Control (Sheet 1)

Because two analog signals are sampled simultaneously, a pointing circuit, consisting of CYCLE 1 and CYCLE 2 flip-flops, is used to point to the A/D samples to be converted. Initially, CYCLE 1 and CYCLE 2 are both in the clear state. When an A/D start command is initiated, the CYCLE 1, HOLD, and HOLD SAVE flip-flops are set, and the HOLD flip-flop starts the A/D conversion. The first sample to be converted is pointed to by the signal CH2H, which is created by the CYCLE 2 flip-flop.

When an A/D conversion is initiated by the A/D control, both sample-and-hold modules simultaneously hold the analog input. Sample-and-hold 1 monitors channels 0–7, and sample-and-hold 2 monitors channels 10–17. When a channel from 0 to 7 is selected, a corresponding channel from 10 to 17 is monitored by sample-and-hold 2 (0 and 10, 1 and 11, etc.). The first value converted will be the sample from sample-and-hold 1. The program must initiate a second A/D conversion to convert the analog value held by sample-and-hold 2. The signal on sample-and-hold 2 is held for 75 μs before droop becomes apparent, so the second conversion must begin as soon as possible after completion of the first one. (Refer to the *LPS11-S User's Guide* for programming details.)

At the completion of the A/D conversion, the EOCP signal clears the CYCLE 1 flip-flop (DMA and BUSRT MODE) and conditions the A/D control to prepare for the second conversion by setting the CYCLE 2 flip-flop (Figure 3-20). The EOCP signal clears the HOLD flip-flop, and the HOLD SAVE flip-flop remains set. If the interrupt is enabled, the DONE signal nofitifes the processor that the conversion is complete, and that the software should read the A/D buffer.

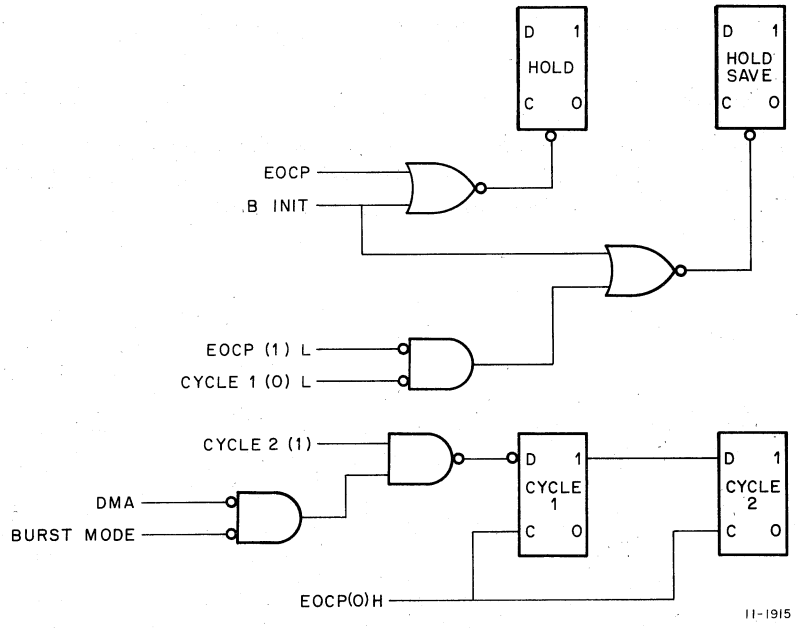

Figure 3-20 Dual Sample-and-Hold Control (Sheet 2)

After the first sample value has been read from the A/D buffer, the second sample is ready for conversion and the A/D control waits for another A/D start command, which sets the HOLD flip-flop and starts the conversion. At the completion of the second sample conversion cycle, the CYCLE 2 and HOLD SAVE flip-flops are cleared, leaving the A/D converter ready for the next dual sample-and-hold conversion process. Figure 3-21 illustrates dual sample-and-hold timing.

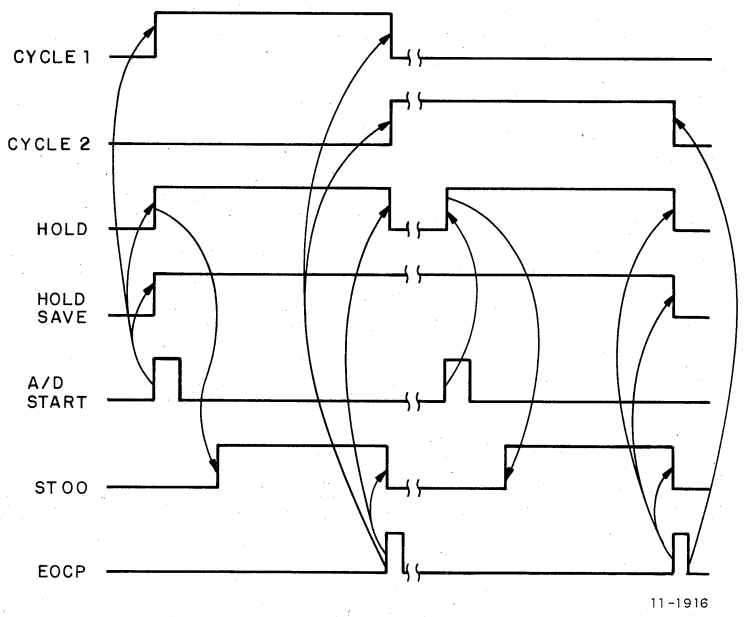

Figure 3-21 Dual Sample-and-Hold Timing

3.2.10 Analog Components

3.2.10.1 A241 or A242 Preamplifier – Two types of preamplifiers may be used in the LPS11-S. The first, designated LPSAG, converts a ±1V input to a ±5V output. The second, designated LPSAG-VG, is individually selectable for each of its four channels, which can accept inputs of ±1V, 0 to +2V, ±5V, or 0 to +10V.

Each type is composed of four differential amplifiers that use negative feedback to amplify the difference in the voltage inputs. When amplifier output changes due to a voltage level deviation at one of the corresponding amplifier inputs, a portion of the output is fed back to the input, tending to cancel the change. The value of the resistors employed in the feedback path determines the input/output ratio and, consequently, the amplifier gain. In the case of the LPSAG, the resistors are fixed so that the output will always be 5 times the amount of the differential input voltage. The LPSAG-VG contains selectable jumper modules that select alternate resistance configurations in the amplifier feedback path. This changes the amount of feedback and thus the gain of the differential amplifier.

Each differential amplifier contains its own gain, balance, and common mode rejection controls. The gain potentiometer enables the user to vary the differential amplifier feedback voltage to obtain the desired output. The balance potentiometer enables the user to adjust the amplifier to ensure that the output is 0V in the absence of an input signal. The common mode rejection control is used to maximize the input common mode noise attenuation level.

3.2.10.2 A407 Multiplexer – The LPSAD-12 contains a single multiplexer, which provides 8 channels to process analog input signals from external devices. This 8-channel capacity can be expanded to 16 channels by the addition of a second 8-channel multiplexer (LPSAM). The 16 channels resident in the LPSAD-12 are designated 00–17.

Multiplexer selection is determined by connecting the appropriate output jumper on IC E2 (see drawing D-CS-A407-0-1, sheet 2), causing a low to be applied to IC E4 pin 12. Channel selection is determined by the signals MUX 3L, MUX 4L, and MUX 5L, which decode the channels selected by the E2 jumper connections, causing one of the eight E4 outputs to assume a low state. The selected output applied to the base of a corresponding transistor (Q10–Q18) causes the transistor to conduct, thereby enabling one of the analog channels.

The analog input signals, designated SIG CH0 through SIG CH7, are applied to eight corresponding field-effect transistors (Q1–Q8). These FETs are turned on when the gate voltage is selected to a positive level, and are turned off when the gate is selected to a negative level.

When the FET conducts, the drain-to-source characteristics appear as a short circuit, so that any voltage applied at the drain appears at the source. The source voltage is applied to E1 pin 5, which is used as a buffer amplifier. E1 has a very high input impedance and a low output impedance. The selected MUX output, designated MUX 1 OUT, appearing at E1 pin 10 is applied to the sample-and-hold module for subsequent processing.

Transistors Q19 and Q20 form an emitter follower, which lowers the output at E1 pin 10 by 0.7V. Diodes D23 through D31 clamp the gate level at 0.7V higher than the output of the emitter follower, so that the gate voltage of the conducting FET is maintained within a few millivolts of the drain and source voltage.

The 8-channel multiplexer actually contains nine channel circuits, eight of which are used to process analog signals from external devices. The ninth channel, the expander input channel, is not utilized in any present LPS11-S configurations. Each of the analog input channels contains a 47Ω fusible resistor, which provides overvoltage protection for the multiplexer circuits.

Note that only one E2 jumper can be installed at a time. Only one jumper, 00–07, is installed on the basic LPSAD-12 multiplexer module. When an additional multiplexer is used, jumper 0–7 ONLY must be removed from all other multiplexer modules.

3.2.10.3 A406 Sample-and-Hold – The sample-and-hold circuit operates in two modes to process data from the selected multiplexer channels for subsequent conversion by the A/D converter. When operating in the sample mode, the circuit converts the multiplexer input (±5V) to a 0–10V output, which is applied to the A/D converter and converted into an equivalent digital output. When a hold signal is initiated, the last output voltage is remembered until the A/D converter finishes its conversion and is ready to accept new data. At this time, the A/D control signals that the hold function is no longer required, and the circuit reverts to the sample mode of operation.

When a single sample-and-hold configuration is employed in the LPSAD-12, signal HOLD L is absent from E7 in the sample mode of operation (see drawing D-CS-A406-0-1). Transistors Q1 and Q2 form the operating mode selection switch. In the absence of HOLD L, the base of Q1 is maintained at +5V, while the base of Q2 is held at 1.4V by diodes D9 and D10. The emitters of Q1 and Q2 are at approximately +2V. As a result, Q1 is back-biased (turned off) and its collector voltage is clamped at approximately -9V by diodes D3 and D4, while Q2 is turned on. As Q2 conducts, its collector voltage tends to rise toward the emitter level, but is clamped at zero volts by diode D6. The resultant output voltages developed at the collector of Q1 and Q2 are -9V and 0V, respectively.

The collector voltages of the mode selector transistors are applied to four field-effect transistors (Q6 through Q9), which act as switches to gate or store the multiplexer output data. To turn on these transistors, the gate voltage source must be driven close to 0V. Conversely, the transistors are turned off when the gate-to-source voltage is driven negative; in this case, -9V.

With transistor Q1 cut off and Q2 conducting in the sample mode of operation, the collector voltage of Q1 (-9V) is applied to the gate input of Q8 and Q9, biasing these transistors off, while the collector voltage of Q2 (0V) is applied to the gate inputs of Q6 and Q7, causing them to conduct. Signal MUX 1 OUT from the selected multiplexer channel is added to the OFFSET input from the A/D converter and applied through Q7 to an inverting amplifier with high input impedance, high speed, and high gain operating characteristics. Capacitor C17 is grounded through Q6. Feedback through R24 sets the output, S&H X OUT at 0 to -10V, corresponding to ±5 to +5V at MUX 1 OUT.

In the hold mode of operation, signal HOLD L is applied through E7 to the base of Q1, dropping the +5V level to approximately +0.2V. This turns on Q1, which, in turn, effects the biasing of Q2, turning it off. The effect is to reverse the respective collector voltages of Q1 and Q2, causing the associated FETs to reverse their state of conduction. Transistors Q8 and Q9 are turned on, and Q6 and Q7 are turned off. Capacitor C17 remains charged to the last voltage that was output in the sample mode. Capacitor C17 is connected through Q9 to the input of the S&H amplifier, so that the voltage previously appearing on C17 now appears at the OUT terminal of the amplifier. The function of Q8 is to ground the input leads at R2 and R1 to prevent leakage across Q7 from entering the amplifier.

Transistor Q10 functions as an output switch. Its operation provides for the incorporation of a second sample-and-hold module (dual sample-and-hold function) in the LPSAD-12. When signal CH 1 H is high, transistor Q3 is turned off, causing the anode of diode D15 to become negative and turning on Q10. Similarly, the output switch of the second sample-and-hold module is turned off, feeding the appropriate S&H 1 data to the A/D converter for processing. When CH 1 H is low, Q3 is biased on. D15 becomes forward-biased as the signal at OUT is the range of 0–10V. The voltage drop across R18 causes Q10 to turn off, enabling the second sample-and-hold output.

The potentiometer reference voltage circuit provides signals POT -1, POT +1, POT +5, and POT -5 for use by the four front panel potentiometers of the LPS11-S, which are used to establish program parameters.

Diodes D19 and D20, together with resistors R31, R32, R39, and R40, divide the + and -15V input to produce the + and -5V and + and -1V reference sources. Amplifers E3 through E6 serve as buffers to prevent the Zener diodes from being damaged by transients appearing when phone plugs are inserted into the jacks corresponding to the four potentiometers. Amplifier E5 feeds transistor Q11, which serves as a current supply to drive the potentiometers. Input to E5 is provided by diode D19 and R37, while the output of E5 is applied to the base of Q11, turning it on. The collector of Q11 supplies current to the potentiometers through voltage protection diode D21. The +5V supplied to the potentiometer via signal POT +5 is sensed through R36 and fed back to E5-3 for regulation. POT -5 operates in a similar manner. (A load must be connected between POT +5 and POT -5 for proper operation of these circuits. Signals POT +1 and POT -1 are used for the ±1V preamplifier range of LPSAG or the ±1V and 0 to +2V range of the LPSAG-VG preamplifier option. These signals function in a manner similar to POT +5 except that the transistor is replaced by current limiter R42 or R20. The input to E4 and E6 is derived from the 5:1 voltage divider on the Zener diodes. A load is not required to maintain these reference voltage circuits in an operational mode.

3.2.10.4 A804 A/D Converter – The A/D converter module is an 8- to 12-bit, successive approximation converter containing a PC rotary switch by which the word length may be selected. Operation is unipolar (0 to -10V FS). A stable +5 Vdc output is provided for offsetting a preamplifier or sample-and-hold half scale to achieve bipolar operation. Table 3-9 shows module A804 coding.

Table 3-9
A804 Coding

Code MSB – LSB	Input
1 – 1	-(10–1 LSB) Vdc
10 – 0	-5 Vdc
0 – 0	0 Vdc

Three manual adjustments are provided: a 200Ω gain trim potentiometer, a 2K zero offset potentiometer, and a 25K conversion time adjustment. The period of the internal clock decreases during conversion to provide more time for the MSBs to settle than for the LSBs, thus optimizing the D/A settling time.

Basically, all successive approximation A/D converters consist of:

- A clock or timing chain to establish each bit interrogation time.
- A sequencer to establish the order in which the bits are interrogated (usually MSB to LSB). Timing chains (single shots in tandem) also serve as sequencers.
- A holding register to retain the result of each bit interrogation, and to hold each D/A bit that is accepted.
- A D/A converter, the output of which is compared against the analog input during the conversion.
- A voltage comparator to compare the D/A output against the analog input. The comparator output is fed into the data line of the holding register where the result is stored.

In the A804 module, conversion is initiated by a high-to-low transition at $\overline{\text{START CONV}}$ when ENABLE CONV is high. (Figure 3-22 is a simplified block diagram of the A804; for a more detailed version, see drawing D-CS-A804-0-1.) A +3 Vdc output is provided to tie ENABLE CONV high when gating of $\overline{\text{START CONV}}$ is not desired. The timing requirements are shown in Figure 3-23.

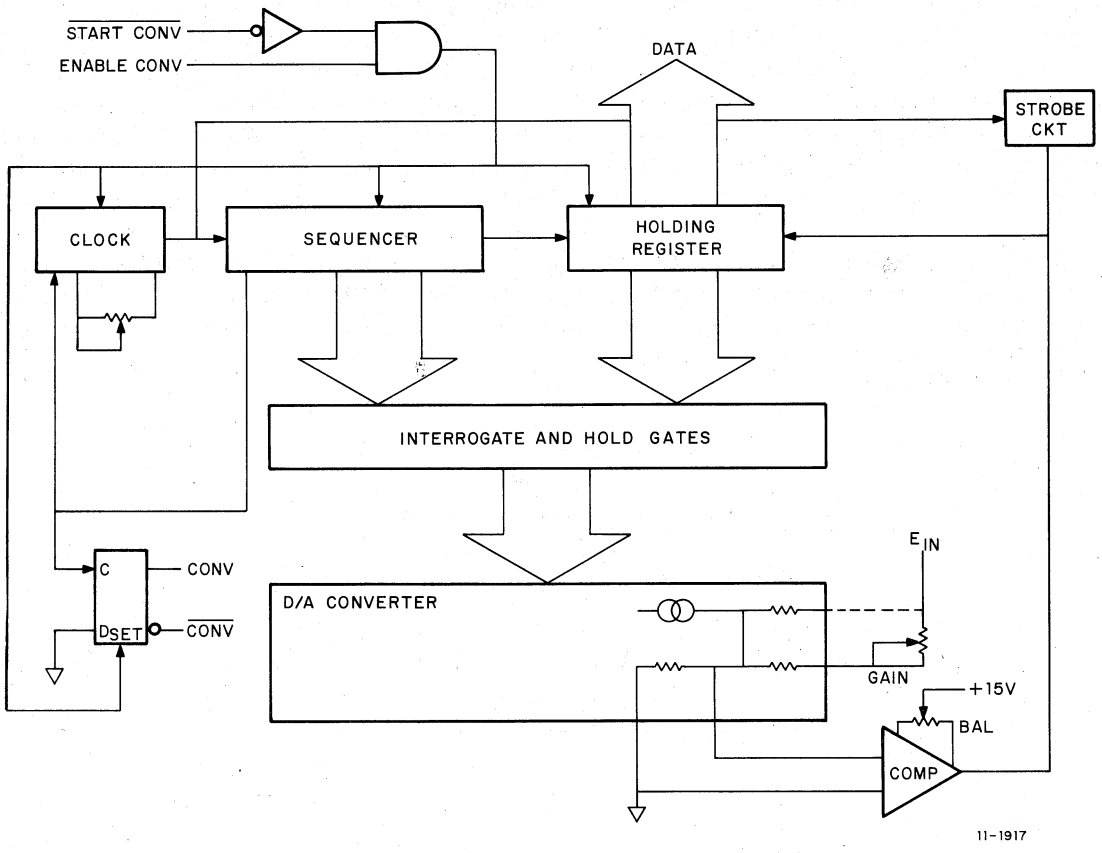

Figure 3-22 A804 Simplified Block Diagram

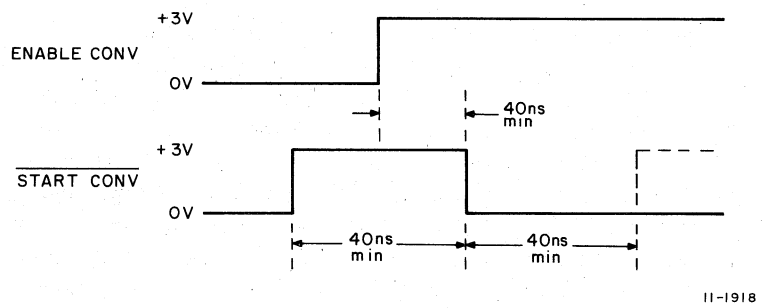

Figure 3-23 A804 Timing Requirements

If ENABLE CONV goes high while $\overline{\text{START CONV}}$ is low, a conversion will also be initiated. The actual conversion is delayed 200 ns to ensure adequate time for the clock to reset. The CONV output goes high within 65 ns and $\overline{\text{CONV}}$ goes low within 80 ns of the $\overline{\text{START CONV}}$ initiation transition. Both CONV and $\overline{\text{CONV}}$ remain asserted during conversion, and terminate at the end of conversion.

The sequencer is a 12-bit shift register through which one "0" is shifted from the MSB to each bit in sequence. The sequencer outputs are ORed with each of the corresponding holding register outputs to the D/A converter inputs. The sequencer interrogates each D/A bit in order, starting with the MSB. At the end of each interrogation, the holding register is clocked to accept or reject the bit. That decision is arrived at by summing the currents of the D/A converter output and the analog input, which are of opposite polarity, so that the current sum actually represents the difference between the two. The voltage resulting from a current imbalance is fed into a voltage comparator referenced to common, and the output of the comparator is tied back to the common DATA line of the holding register. If the interrogated D/A bit supplies more current than the analog input removes, the result is a positive voltage and the bit is rejected; i.e., "0." If the result is a negative voltage, the bit is set to "1." In this way, the converter zeroes in on the correct value, providing a more accurate approximation with each successive decision.

The PC rotary switch connects the last desired bit of the sequencer to the clock input of the CONV status flip-flop and the data input of clock control flip-flop. When the connected bit interrogation terminates, the decision is clocked into the holding register, the clock is inhibited, the CONV status flip-flop is complemented, and the sequencer is loaded with all "1s," indicating the end of the conversion.

A special strobe circuit connected to the output of the comparator allows the comparator decision to be available for only 100 ns, preventing stray feedback from propagating through and affecting the final result.

3.2.10.5 A408 Switched Gain Multiplexer – The A408 contains a single multiplexer and programmable gain amplifier which provide 8 channels and 4 different gains (1, 4, 16, 64) to process analog input signals. This 8-channel capacity can be extended to 16 channels by the addition of a second 8-channel switched gain multiplexer (LPSAM-SG). When using the A408s in place of the A407s, the 16 channels which make up the LPSAD-12 will be designated as follows:

Address	Result
Channels 0–17	Channels 0–17 at G=1
Channels 20–37	Channels 0–17 at G=4
Channels 40–57	Channels 0–17 at G=16
Channels 60–77	Channels 0–17 at G=64

Multiplexer selection is determined by attaching W2 in the appropriate position ("0–7" or "10–17"). Channel selection is determined by the four MUX signals, MUX 0 L, MUX 1 L, MUX 2 L, and MUX 3 L. If the module is to be used for channels 0–7, W2 is left in the "0–7" position, so that MUX 3 L is applied directly to pin 1 of the multiplexer chip, IC E1, thereby enabling the multiplexer when MUX 3 is in the 0 state, i.e., MUX 3 L is high (pulled up to +10 V). If the module is to be used for channels 10–17, W2 is moved to the "10–17" position, so that the inverted MUX 3 L is applied to pin 1 of the multiplexer chip, thereby enabling the multiplexer when MUX 3 is in the 1 state, i.e., MUX 3 L is low. MUX 0 L, MUX 1 L and MUX 3 L are applied directly to the multiplexer chip to select the desired channel. The low input on these three lines is ground at the module's input pin, clamped by D50, D51 or D52, to +4 V at the multiplexer chip input. If all three are low, channel 7 is enabled; if all three are high (pulled up to +10 V), channel 0 is enabled.

Gain level (1, 4, 16 or 64) is determined by the state of MUX 4 L and MUX 5 L. If MUX 4 L and MUX 5 L are both high (0,0) at the pin 12 and 13 inputs of E5, then E5 pin 11 is low, selecting a gain of 1. If MUX 4 L and MUX 5 L are both low (1,1), high levels result at the pin 1 and 2 inputs of E5, so that E5 pin 3 is low, selecting a gain of 64.

The RTO fine (R24) and RTO coarse (R25) pots are used to adjust for zero at the output of E3 at a gain of 1.

The RTI circuit, consisting of Q3, Q2, R22 and associated components, is used to adjust for zero at the output of E3 at a gain of 64.

E2 and E6 are 1-of-4 multiplexers. E2 is used to select the correct resistor value to maintain the amplifier bandwidth constant at the different gains. E6 is used to select the correct voltage level to be fed back to the input of E3. The feedback ratios for the 4 different gains are determined by the resistor divider network consisting of R37–R42.

Each of the analog input channels contains a 47-ohm fusible resistor and two clamping diodes, which provide over-voltage protection for the multiplexer circuits.

3.2.11 Direct Memory Access (DMA)

The LPSAD-NP DMA option is used only in conjunction with the LPSAD-12. DMA adds additional speed to the A/D conversion process by storing A/D conversions in memory without program intervention. The LPSAD-12 and LPSAD-NP can operate in four modes of operation: single conversion, dual sample-and-hold, single burst, or dual sample-and-hold burst modes.

3.2.11.1 DMA Programming – A/D Status register bits 02 and 01 are used to point to the DMA registers (Figure 3-24), which consist of Status, Word Count, and Current Address registers with associated control and timing circuits.

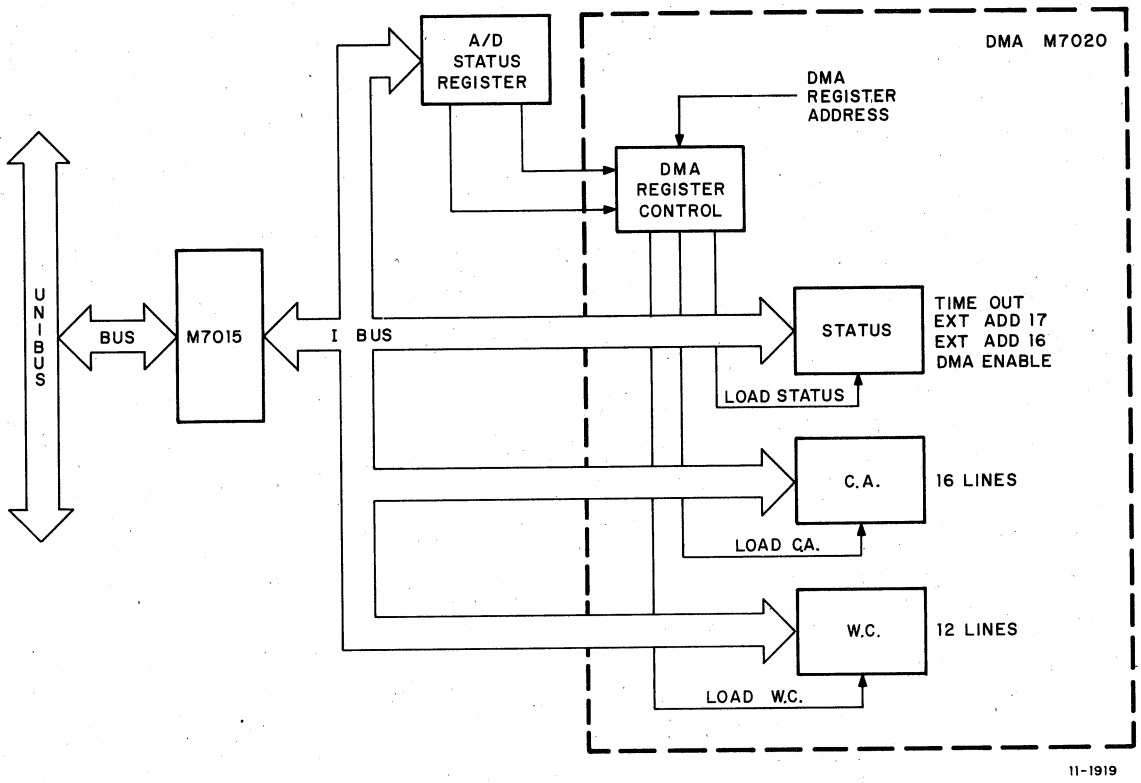

Figure 3-24 DMA Register Control Block Diagram

To address the DMA registers, it is first necessary to address the A/D Status register and supply the proper bit configuration for bits 02 and 01, (as shown in Figure 3-25 and described in Table 3-10), after which the DMA Status register may be addressed (Figure 3-26 and Table 3-11).

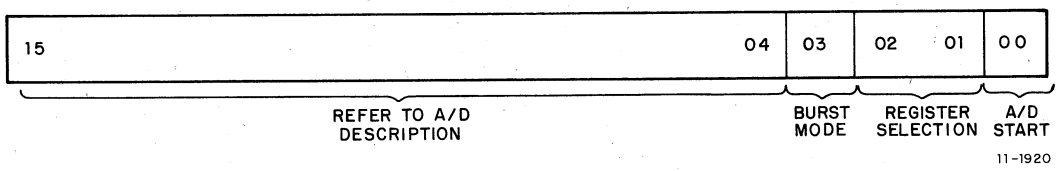

Figure 3-25 A/D Status Register DMA Bit Assignments

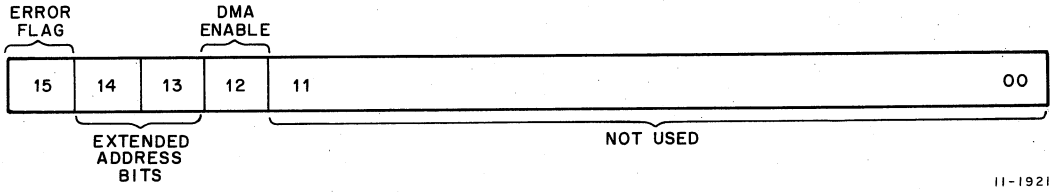

Figure 3-26 DMA Status Register Bit Assignments

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Table 3-10
A/D Status Register Illustrating DMA Bit Functions

Bit	Name	Function
15–04	Refer to A/D description	
03	Burst Mode	When set, allows the A/D to do conversions at the maximum rate of the converter, with a restart at the end of each conversion until WC overflow.
02–01	DMA register selection	**02 01 Register** 0 0 N/A 0 1 DMA status 1 0 DMA word count 1 1 DMA current address
00	A/D start	Program A/D converstion starts

Table 3-11
DMA Status Register Bit Functions

Bit	Name	Function
15	Time Out Error	When set, a time out error has occurred.
14–13	Extended Address Bits	**14 13 Core** 0 0 32K 0 1 64K 1 0 96K 1 1 128K
12	DMA Enable	When set, allows the DMA to transfer A/D conversions into core without processor intervention.
11–00	Not Used	

The Word Count register contains the 2's complement of the number of transfers to be performed. At the completion of the transfers, the Word Count register overflows (makes the transition from 7777 to 0000) and interrupts the processor. Figure 3-27 shows the bit allocation for the Word Count register.

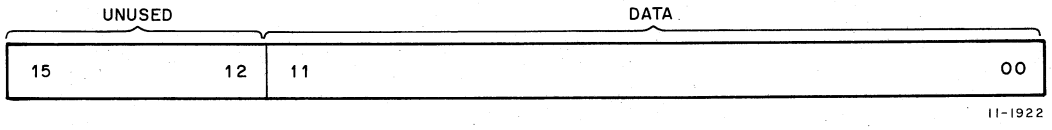

Figure 3-27 Word Count Register

The Current Address register is a 16-bit register that defines the location in core where the data is to be stored. After each transfer, the Current Address register is incremented by two. This register can be loaded with any location in the first 32K of core, but if the user wishes to store data in locations above the first 32K of core, the extended address bits of the DMA Status register must be used (Figure 3-28).

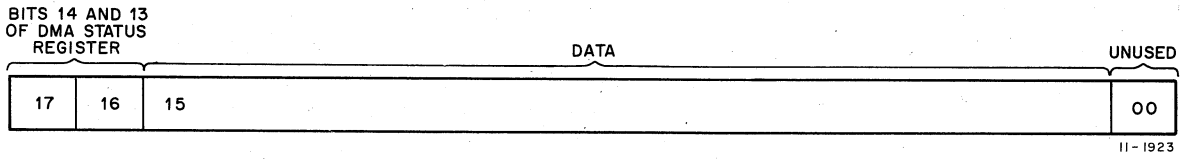

Figure 3-28 Current Address

3.2.11.2 Single DMA Operation – Once initialized, the single DMA operation will, at the completion of an A/D conversion, perform one Non-Processor Request (NPR) cycle. The DMA stores the A/D conversion into memory without program intervention and waits for another A/D start command. To initialize the DMA, the Word Count, Current Address, and Status registers must be loaded. Loading the DMA Status register with bit 12 = 1 sets the DMA flip-flop, enabling DMA operation.

The single DMA operation will only begin upon receipt of an A/D start command, either clock overflow, Schmitt trigger, or program start. From the time the A/D conversion is processed, to the time the EOCP signal is returned by the A/D converter, the A/D conversion process does not differ from a normal error-free A/D conversion.

However, the EOCP, in addition to clocking the SAVE and DONE flip-flops in the A/D control (Paragraph 3.2.7), also clocks the NPR REQ flip-flop in the DMA (Figures 3-18 and 3-29). NPR REQ (1) is ANDed with DFF (0) to produce BUS NPR, informing the processor that an NPR is active and that it should increment the Word Count register.

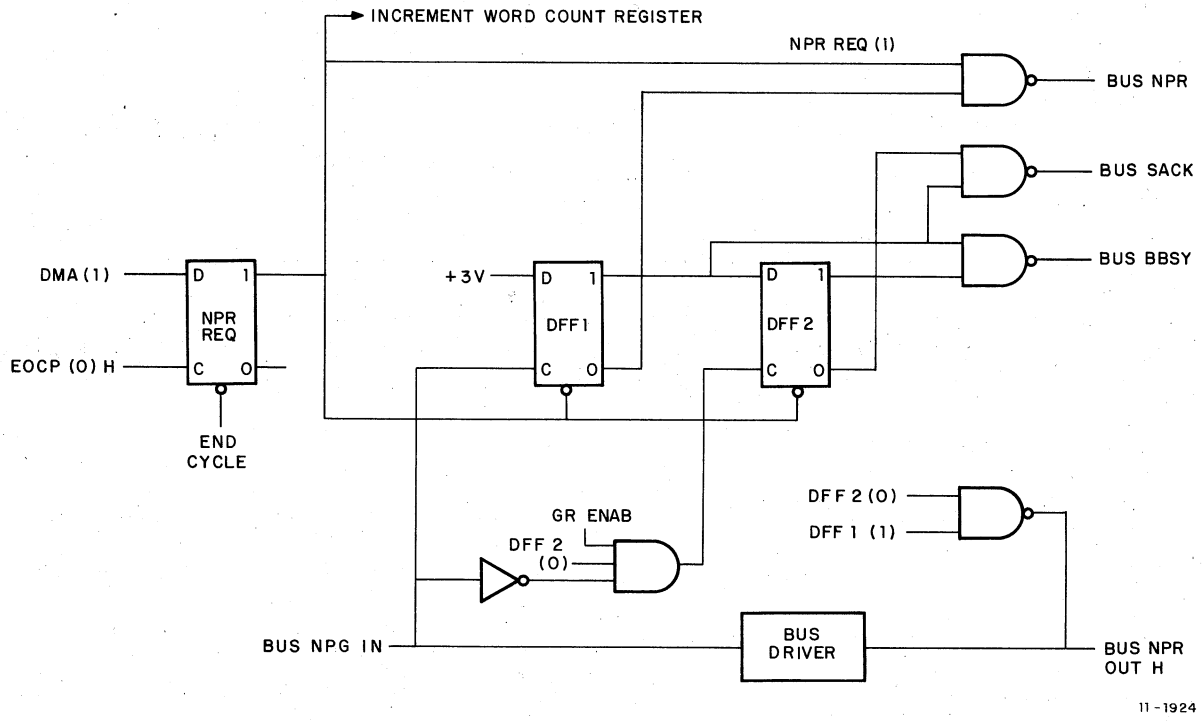

Figure 3-29 DMA Bus Control Logic

During DMA the end of an individual conversion does not result in an interrupt, because it is not significant to the processor. Completion of the entire DMA operation is significant, however, and this is signaled by an overflow of the Word Count register. The processor responds with BUS NPG IN, clocking DFF1 to the "1" state to be ANDed with DFF2 (0) to inhibit BUS NPG OUT from being passed on, thus enabling the DMA to gain control. DFF1 is ANDed with DFF2 to produce BUS SACK (Select ACKnowledge).

The signals GR ENABLE and DFF2 (0) are ANDed with the removal of BUS NPG IN by the processor to clock DFF2 to a "1" state. When DFF2 is set, DFF1 is ANDed with DFF2 to produce BUS BBSY, which informs all devices that the Unibus is busy.

Setting DFF2 also sets the CNTR flip-flop (Figure 3-30), which simultaneously generates several functions. Signals ADDR BUS LOW and ADDR BUS HIGH place the current address on the Unibus. The signal DATA BUS, generated by CNTR, creates the signal DATA BUF IN (Figure 3-31); DATA BUF IN gates the contents of the A/D buffer onto the internal bus D15:D00 and direct clears the SAVE and DONE flip-flops to inform A/D control that the A/D buffer has been read (Figure 3-18). DATA BUS is also sent to the bus control module, generating the IN signal, which gates I BUS D15:D00 (the contents of the A/D buffer) onto the Unibus.

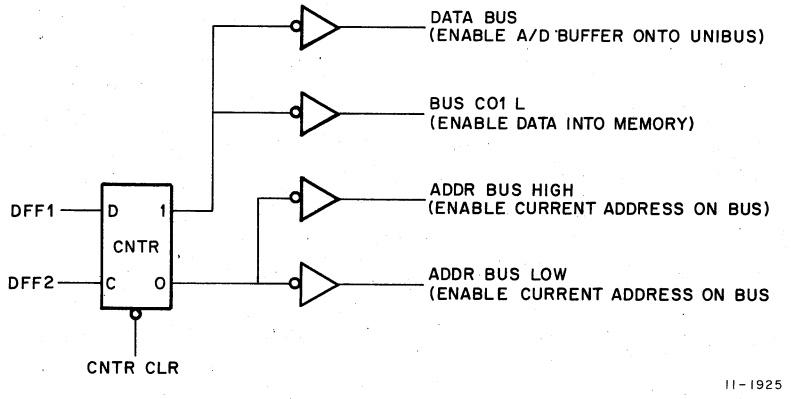

Figure 3-30 Functions of the CNTR Flip-Flop

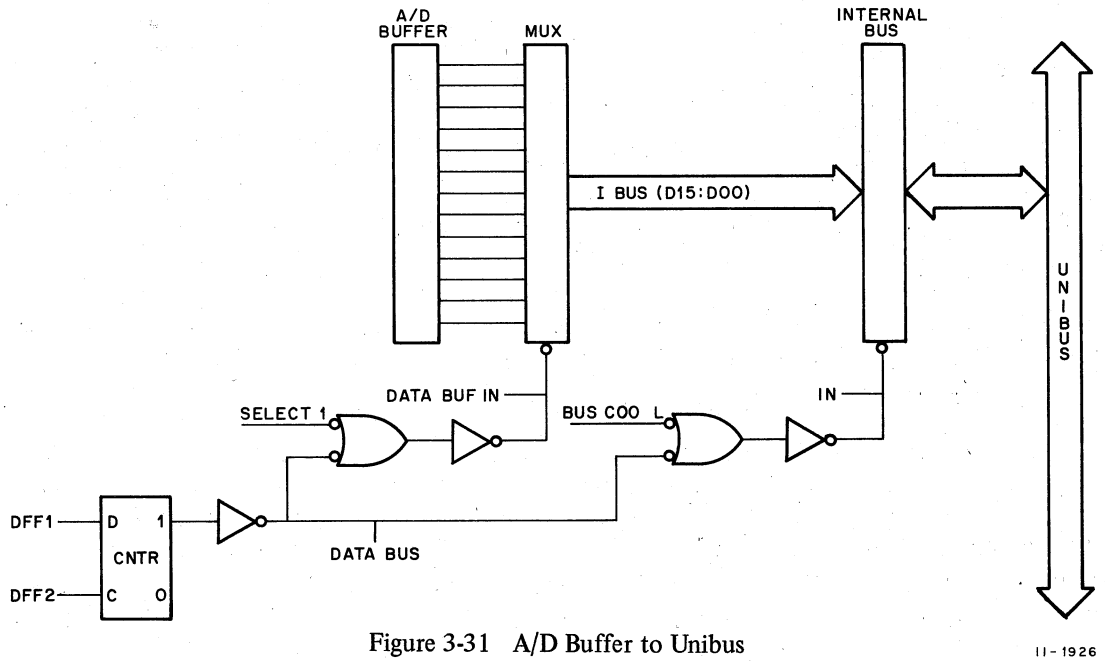

Figure 3-31 A/D Buffer to Unibus

The CNTR flip-flop also generates the signal BUS C01 L, which informs memory that the direction of data flow is into memory, and triggers the DESK (Deskew) 150 ns delay (Figure 3-32). Thus, the data and address lines are allowed to settle before memory reads the bus by setting the MSYN flip-flop.

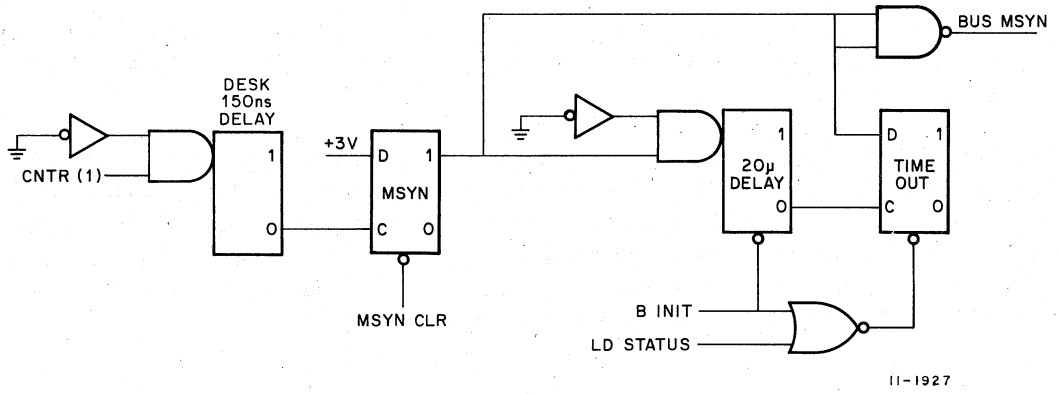

Figure 3-32 Generating MSYN

When the data has been received, memory responds with BUS SSYN to the bus control, which generates SYNC to the DMA. SYNC is ANDed with CNTR (1), creating MSYN CLR to clear MSYN (drawing D-CS-M7020-0-1, sheet 3), with CNTR CLR being generated 100 ns later to clear CNTR.

Clearing the MSYN flip-flop disables the TIME OUT flip-flop, indicating that the transfer has occurred within the prescribed 20 μs limit. If the data had not been received by then, SYNC would not have been generated in time, and the TIME OUT flip-flop (Error flag bit 15 of the DMA Status register) would have been set, disabling DMA.

When the CNTR flip-flop is cleared by CNTR CLR, a 100 ns pulse creates the signal END CYCLE, which clears the NPR REQ flip-flop and increments the Current Address register. When the NPR REQ flip-flop is cleared, it direct clears the DFF1 and DFF2 flip-flops.

In the single-word DMA transfer mode, if no word count overflow occurs, the A/D control reverts to the ready state and waits for another start command. Figure 3-33 shows single-word DMA transfer timing.

3.2.11.3 Dual Sample-and-Hold DMA Operation – When the A/D Status register is programmed for a dual sample-and-hold operation (bit 14 of the Status register set), the first A/D conversion must be initiated by a normal A/D start command. The DMA transfers one conversion into memory without program intervention as described above for the single DMA mode. However, in the dual mode the DMA automatically starts the second conversion while the first one is being read into memory.

When the first conversion is complete, BUS NPR becomes true and the processor replies with BUS NPG, setting the DFF1 flip-flop. As the DMA prepares to transfer the first conversion, it simultaneously qualifies the A/D control to convert the second sample (Figure 3-34).

Setting the DFF1 flip-flop qualifies the RES (100 ns) one-shot multivibrator in the A/D control. (For a more detailed illustration, see drawing D-CS-M7018-0-1, sheet 2.) The RES signal is ANDed with the GO signal to set the HOLD flip-flop and start the second conversion process, which proceeds as described in Paragraph 3.2.7. Each subsequent conversion is handled in the same manner until a word count overflow occurs. (The word count must be loaded with an even number.) The A/D control then waits for another start command to be generated by either program start, clock overflow, or Schmitt trigger firing.

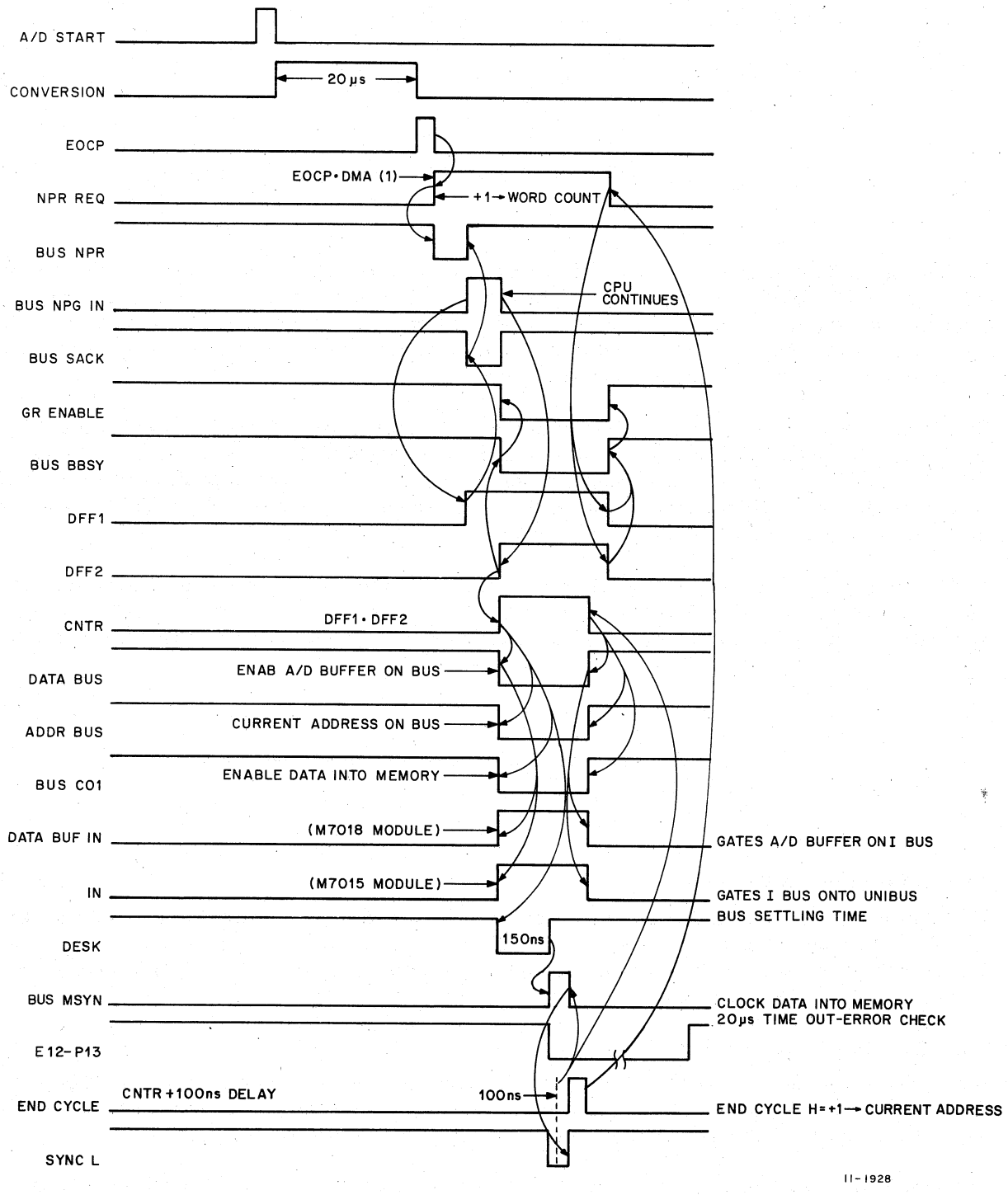

Figure 3-33 Single DMA Transfer Timing

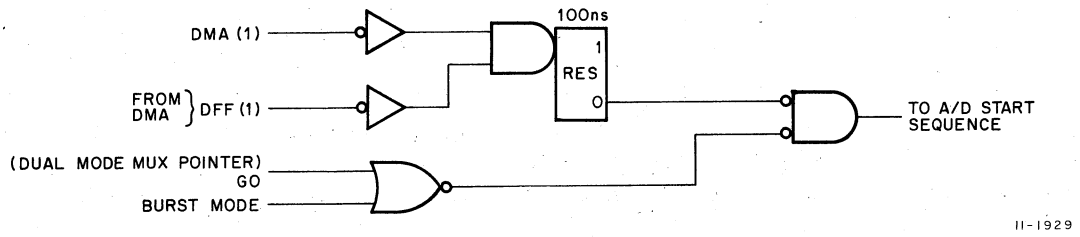

Figure 3-34 DMA Dual Sample-and-Hold A/D Conversion Start

3.2.11.4 Single Burst Operation – If the A/D control is programmed for burst mode (bit 3 of the A/D Status register set) and the DMA is enabled, the first A/D conversion must be initiated by an A/D start command, and is transferred into memory without program intervention just as in single DMA operation. In single burst mode, however, the DMA automatically restarts the remaining conversions until the word count overflows, interrupting the processor to indicate that the DMA operation is completed.

The automatic A/D restart is accomplished much as in dual sample-and-hold mode (Figure 3-34). When DFF1 is set, the RES one-shot multivibrator is ANDed with the BURST MODE signal to start the subsequent conversions, rather than with the GO signal, as in the dual sample-and-hold mode. A new A/D start is generated each time the DFF1 flip-flop is set, until the Word Count register overflows and interrupts the processor. The single burst mode is the fastest rate for acquiring data on a single analog channel.

3.2.11.5 Dual Sample-and-Hold Burst Operation – If the A/D control is programmed for burst mode and dual sample-and-hold operation (bits 3 and 14 of the A/D Status register set) and the DMA is enabled, the first A/D conversion must be initiated by an A/D start command. The remaining conversions are automatically started by the DMA.

NOTE
Unless the word count is an even number, the last conversion will be lost.

3.3 LPSKW REAL-TIME CLOCK

The programmable LPSKW real-time clock provides the user with an accurate method of measuring and keeping time. The clock can be used to synchronize the program to external events, count external intervals, measure intervals of time between events, or provide interrupts at programmable intervals. It also provides two methods of starting an analog-to-digital conversion.

3.3.1 Block Diagram Discussion

The block diagram shown in Figure 3-35 illustrates the various clock circuits, bus control, and the PDP-11 Unibus. The bus control decodes the real-time clock addresses and processes all of the input/output control signals between the clock and the CPU. Paragraph 3.1 is a detailed description of how the bus control operates.

The Read/Write Status register (Figure 3-36) is used to program clock functions, including rate selection, mode control, enabling the internal clock, enabling interrupts, and storing flags. The clock rate selection circuit enables the user to select one of seven rate frequencies determined by the rate bits in the Clock Status register. The rate frequencies are derived from either an internal crystal-controlled oscillator, the power supply line frequency, or Schmitt trigger #1. The Schmitt triggers permit the user to control certain clock operations from external sources.

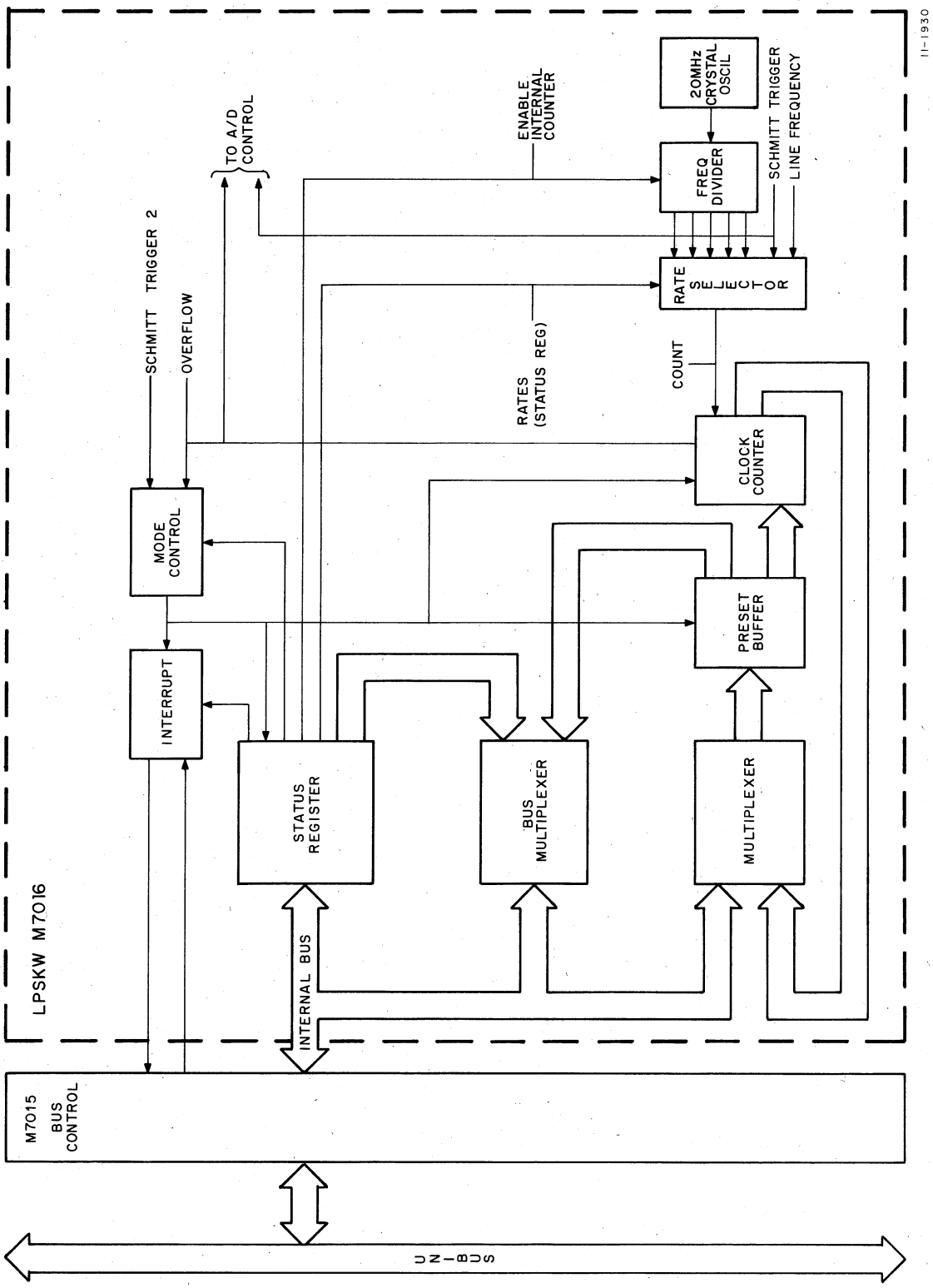

Figure 3-35 LPSKW Clock Block Diagram

15	14	13	12	11	10	09-08	07	06	05-04	03-01	00
STI FLAG	STI INT ENABLE	STI ENABLE	MAINT STI	MAINT COUNT	MAINT ST2	MODE	MODE FLAG	MODE INT ENABLE	UNUSED	RATE	CLOCK ENABLE COUNT

11-1931

Figure 3-36 Clock Status Register Bit Assignments

On program command, the selected clock rate is applied to the clock counter (a binary up counter). During normal operation, the clock counter counts from a preset value until it makes the transition from 177777 to 000000. When it reaches the zero count, an overflow pulse is produced.

An overflow of the clock counter or the Schmitt trigger #2 input can be used in four different modes to measure and keep time. The modes are controlled by bits 8 and 9 of the Clock Status register, as described in Table 3-12.

Table 3-12
Clock Status Register Bit Functions

Bit	Name	Meaning and Operation
15 (Read/Write)	ST1 Flag	Setting of this flag by other than maintenance means signifies that ST1 has fired.
14 (Read/Write)	ST1 Interrupt Enable	When set, a firing of ST1 causes an interrupt.
13 (Read/Write)	ST1 Enable	When set, allows an ST1 firing to enable the counter to count at rates and modes selected.
12 (Write Only)	MAINT ST1	Used to check operation (digital only) of Schmitt trigger #1 circuit. This is a write-only bit.
11 (Write Only)	MAINT Count	When set, this bit allows a signal to pulse the counter, provided that proper rate (1 MHz) is selected. This bit is normally used for CMT purposes.
10 (Write Only)	MAINT ST2	Used to check operation (digital only) of Schmitt trigger #2 circuit. This is a write-only bit. Bit 10 can be used to transfer the contents of the counter to the preset buffer while in Mode 2 or 3, below.
09:08 (Read/Write)	Mode	Controls data flow, interrupts, and clock rates.
		09 08 Function
	Mode 1 Single Interval	0 0 Counter counts from preset value to overflow and stops.
	Mode 2 Repeated Interval	0 1 Counter counts from preset value to overflow, then transfers preset buffer to counter and begins again. Interrupts may occur during this mode.

Table 3-12 (Cont)
Clock Status Register Bit Functions

Bit	Name	Meaning and Operation
	Mode 3 External Event Timing	1 0 The counter is free running, and a pulse from Schmitt trigger #2 transfers its contents to the preset buffer; then it continues counting. At each transfer, a Mode flag occurs.
	Mode 4 Event Timing From Zero Base	1 1 Event timing from zero base mode is the same as the previous mode except that, upon transfer of the counter to the preset buffer, the counter is cleared and the count begins from zero.
07 (Read/Write)	Mode Flag	When set, an overflow from the counter or a Schmitt trigger #2 firing has occurred (depending on the mode of operation).
06 (Read/Write)	Mode Interrupt Enable	When set, an overflow from the counter or a Schmitt trigger #2 firing causes an interrupt (depending on the mode of operation).
05:04		Unused
03:01 (Read/Write)	Rate	Controls the rate of the base frequency. The user may select the following rates: **Bits 03 02 01 — Function (Frequency)** 0 0 0 — No rate selected 0 0 1 — 1 MHz 0 1 0 — 100 kHz 0 1 1 — 10 kHz 1 0 0 — 1 kHz 1 0 1 — 100 Hz 1 1 0 — Schmitt Trigger #1 (external) 1 1 1 — Line (50 Hz or 60 Hz)
00 (Read/Write)	Clock Enable Counter	Enables the counter to count at the rate specified by bits 01–03. If no rate is specified, the clock will not count. This bit can be set by Schmitt trigger #1 and cleared by the overflow in mode 1, above. When this bit is cleared, loading the Preset Buffer register also loads the Counter register. Only the external rate will not be inhibited when this bit = 0.

During a mode operation, the Mode flag in the Clock Status register (bit 7) is set. If interrupts are enabled, they are generated and processed by the bus control, which then notifies the processor. The processor processes the interrupt and notifies the clock that the interrupt has been processed.

3.3.2 Programming

Software control of the real-time clock is exercised by two registers; the Clock Status register (Figure 3-36) and the Clock Preset Buffer register.

The Status register controls all clock operations by defining the manner in which the clock is to be used. This register should be loaded after the preset buffer. All normal program instructions, including byte operations, can be performed on the Clock Status register. The maintenance bits (bits 10, 11, and 12) are write-only bits and will always read back as zeroes, as will bits 05 and 04, which are unused. All other bits are read/write bits.

The preset buffer is a 16-bit, read/write, word-oriented register that is loaded with internal bus data or counter data via a multiplexer. (Internal bus data is normally selected, but the firing of Schmitt trigger #2 causes the Preset Buffer register to read the contents of the counter.)

The Preset Buffer register may be loaded either under program control (if bit 00 of the Clock Status register is cleared) or by Schmitt trigger #2 firing, and should be loaded before the Status register to avoid improper initialization of any function.

The Counter register is a 16-bit register that cannot be addressed directly. It is read by transferring its contents into the Preset Buffer register while in modes 2 or 3, and then reading the preset buffer. The Counter register is loaded by loading the Preset Buffer register while bit 00 of the Clock Status register is cleared.

3.3.3 Timing Logic

The LPSKW real-time clock has a self-contained timing generator to ensure proper sequencing of events. The operation of the timing generator must be understood before the logic can be discussed.

A crystal oscillator circuit (Figure 3-37) generates a 20 MHz square wave, which is applied to a J-K-type flip-flop and divided by two, creating the signal CLOCK OUT. This signal is applied to the clock input of a divide-by-10 counter. Table 3-13 shows the binary counting sequence of the divide-by-10 counter.

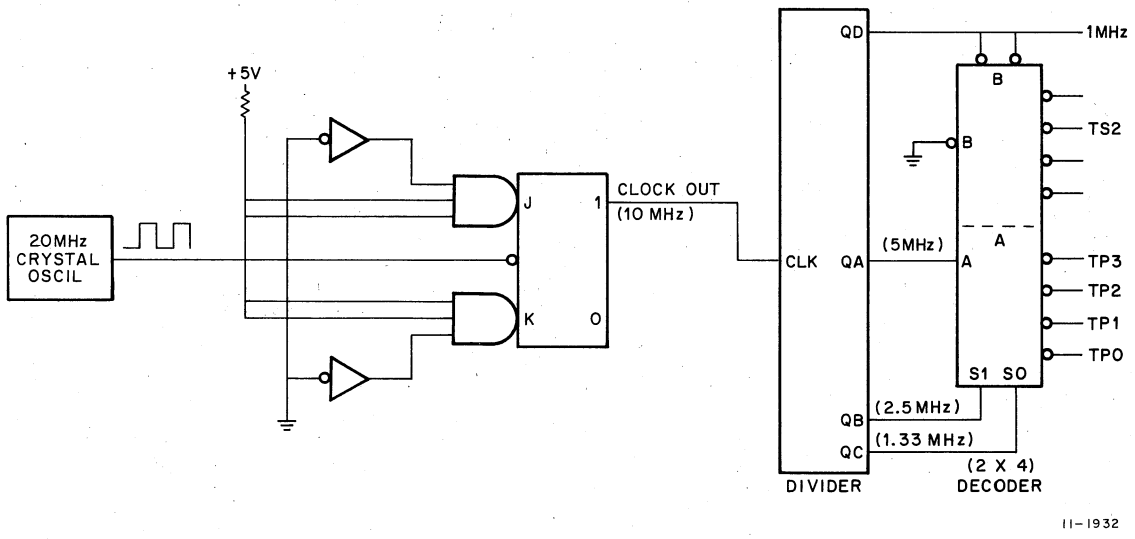

Figure 3-37 Timing Generator

Table 3-13
Divide-by-10 Counter

CLK Pulse 10 MHz	Divide-by-10 Counter Counter Output QD	QC	QB	QA	
0	0	0	0	0	Time state 0
1	0	0	0	1	
2	0	0	1	0	Time State 1
3	0	0	1	1	
4	0	1	0	0	Time State 2
5	0	1	0	1	
6	0	1	1	0	Time State 3
7	0	1	1	1	
8	1	0	0	0	Time State 4
9	1	0	0	1	

The four outputs of the divide-by-10 counter (QA, QB, QC, and QD) are applied to a 2 X 4 decoder, which decodes five time states and five time pulses (Figure 3-38).

NOTE
The LPSKW only utilizes time state 2 and time pulses 0, 1, 2, and 3.

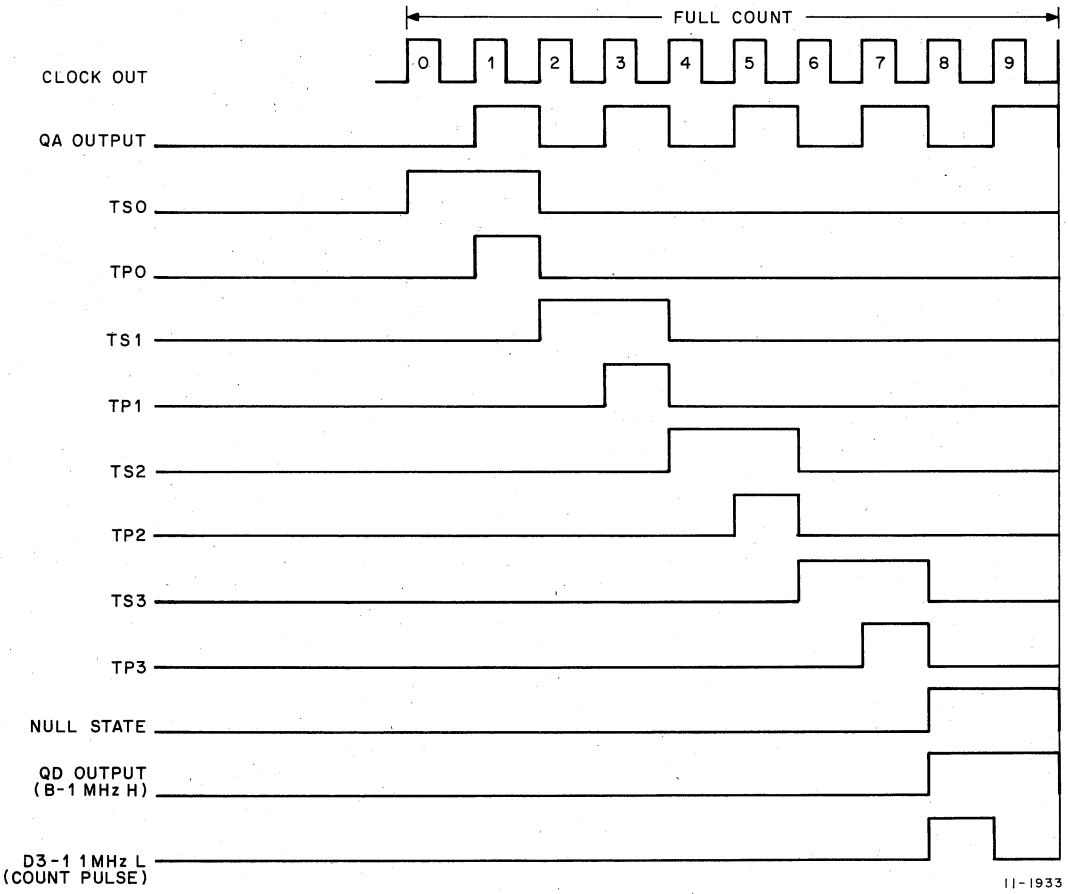

Figure 3-38 Real-Time Clock Timing Diagram

The QB and QC equal a zero state twice in a full-count operation. The TS/TP decoder internally distinguishes the first zero state from the last, ensuring the five time states and five time pulses. The QD output disables the TS/TP decoder during time state 4, causing a null condition. A time pulse is generated during each time state (except the null state) internally in the decoder by ANDing the QA input into one-half of the dual decoder.

3.3.4 Register Addressing

The LPSKW real-time clock is assigned two address select lines (SELECT 2 and SELECT 3) and associated IN/OUT control signals by the bus control. The SELECT 2 line is used only to address the byte-oriented Status register. When SELECT 2 is gated with OUT signals, LD STATUS is generated, permitting byte-oriented data from the processor to be loaded into the Status register (Figure 3-39). When the SELECT 2 signal is gated with the IN signal, RD STATUS permits data to pass through a multiplexer, MUX BUS, and be applied to the Unibus via the internal bus.

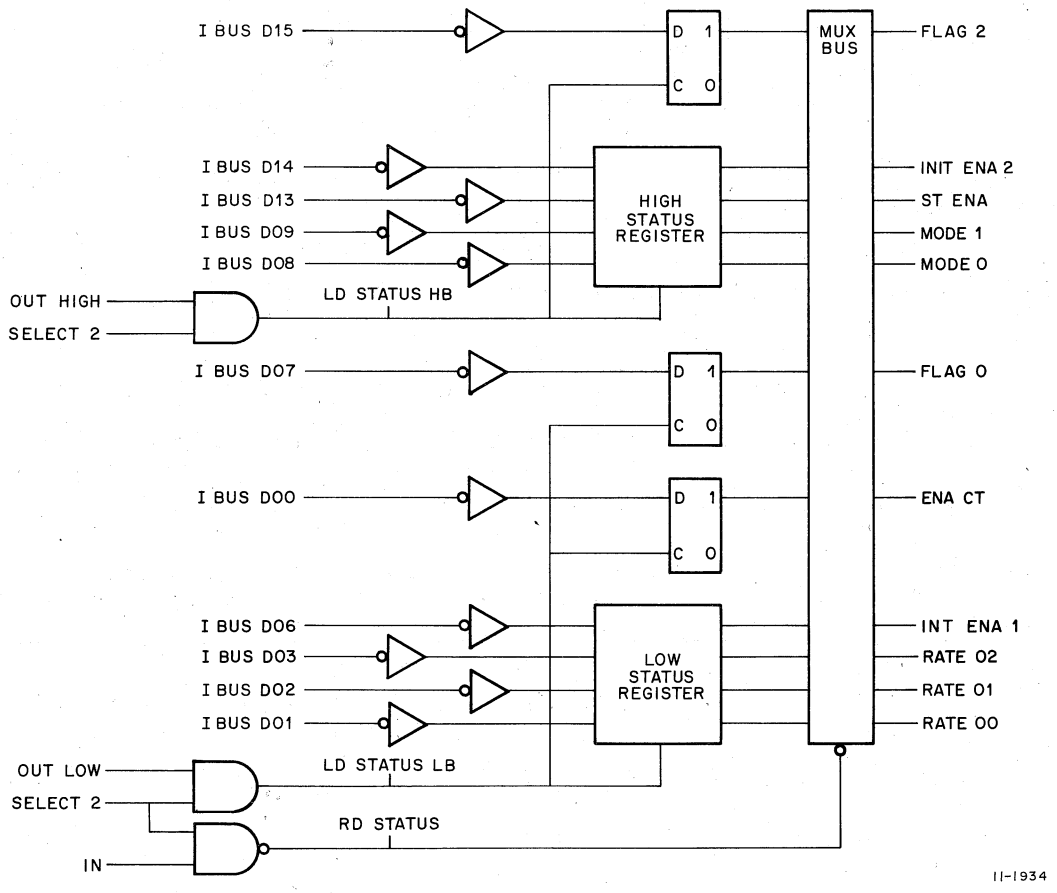

Figure 3-39 Clock Status Register Gating

The SELECT 3 line is used to address the word-oriented Preset Buffer register. Since the preset buffer value should not be in the process of changing during internal data transfers (clock counter transfers), it is necessary to confine the Unibus-to-preset-buffer transfer to a particular LPSKW time state (TS2).

When the processor addresses the Preset Buffer register (Figures 3-40 and 3-41), SELECT 3 is sent to the clock logic, clocking the FF1 flip-flop and releasing the SYNC flip-flop. After the FF1 flip-flop is clocked, the output is inverted and the signal STALL is transmitted to the bus control to inhibit SSYN from occurring. The SYNC flip-flop is clocked at TOP and, in turn, clears the FF1 flip-flop, which releases the STALL signal and allows SYN to be generated.

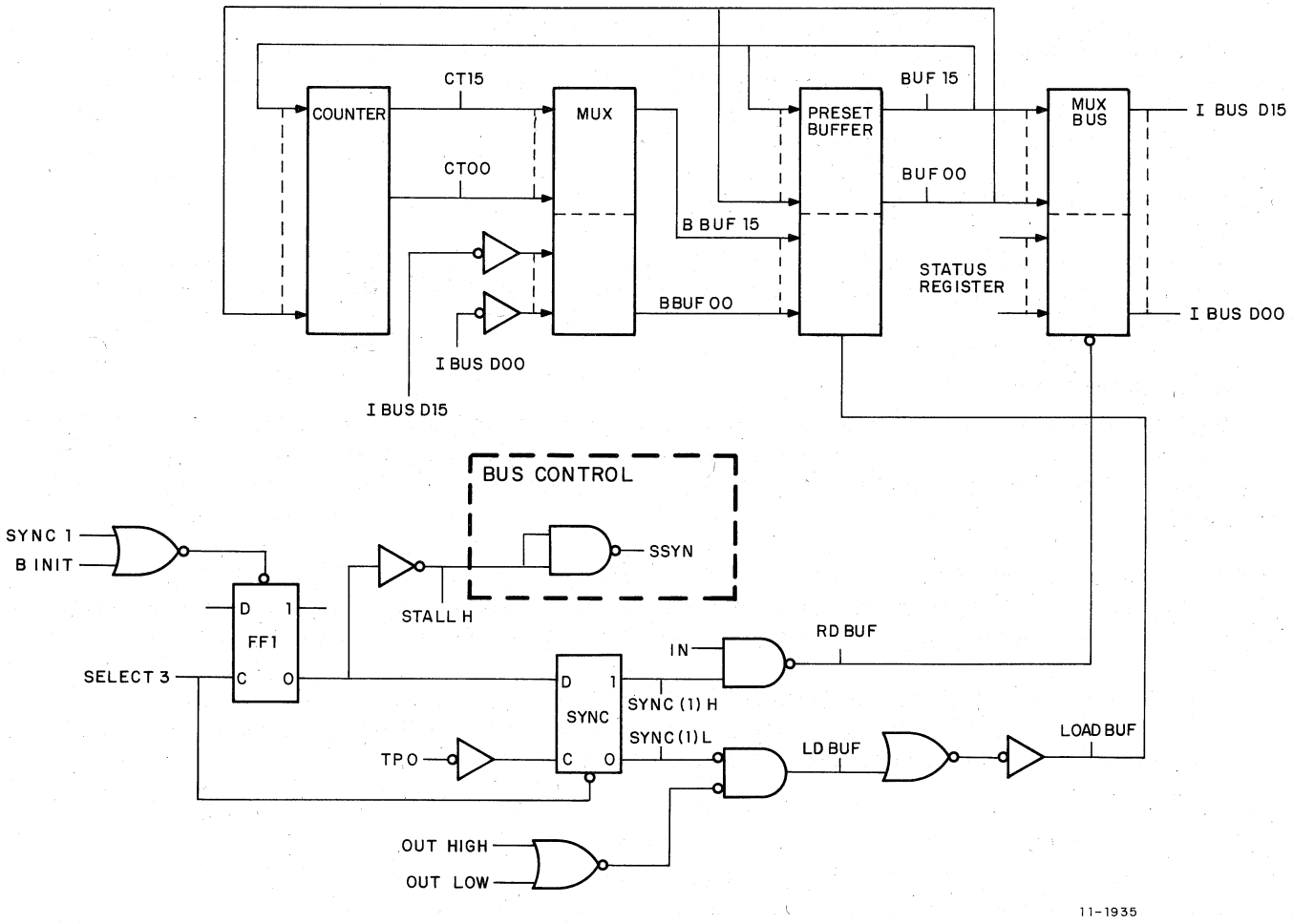

Figure 3-40 Clock Preset Buffer Gating

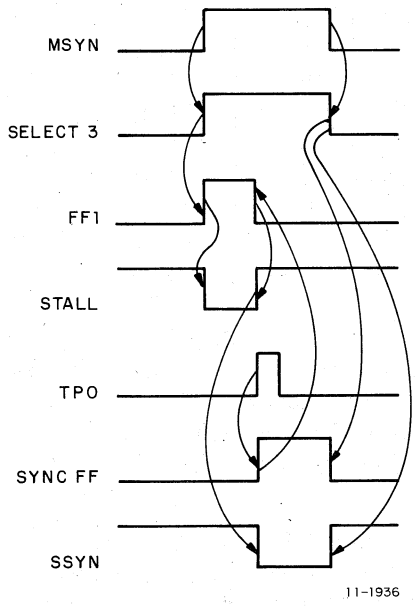

Figure 3-41 Load Operation Timing Diagram

The SYNC flip-flop is gated with the IN/OUT control signals to generate read and write commands. When SYNC is ANDed with IN to generate RD BUF, the contents of the preset buffer are read into the processor. When SYNC is ANDed with OUT (byte-oriented) to generate P LD BUF, the internal bus is loaded into the preset buffer by the signal LOAD BUF. Also, if the counter is not enabled (bit 00 of the Clock Status register), the counter is simultaneously loaded with the contents of the preset buffer.

When the SELECT 3 signal is removed by the processor, the SYNC flip-flop is cleared.

Each of the two select lines generates an I BUS ENABLE RT signal to be used by the bus control to permit a proper master-slave relationship. If the clock is not installed, the processor will time out and trap when using these addresses.

3.3.5 Rate Selection

The LPSKW real-time clock offers seven rates in which to increment the Clock Counter register. Five of the seven rates available are internally generated. Another selectable rate increments the clock counter using the input line frequency. The last rate allows the user to supply an external event. All rates are selected by programming the Status register.

The internally generated rates are enabled when Status register bit 00 is set to a "1." The 1 MHz signal from the timing generator is enabled to ripple through four divide-by-10 counters (Figure 3-42). A 100 ns pulse is generated after each divide-by-10 to provide five selectable rates (1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz).

All of the rates discussed above are applied to a multiplexer. The rate selected depends on Status register bits 01, 02, and 03, which are applied to the multiplexer as signals RATE 0, RATE 1, and RATE 2, respectively. Table 3-14 shows the bit configuration that selects the various rates.

Table 3-14
Clock Count Rates

Status Register Bits			Rate Selected
03	02	01	
0	0	0	None
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	Schmitt trigger #1
1	1	1	Line Input (50 or 60 Hz)

NOTE
Setting maintenance bit 12 of the Clock Status register initiates the same results as the signal ST 1 of the Schmitt trigger #1 circuit; however, this maintenance feature checks only the digital portion of the Schmitt trigger logic.

Only one frequency, 1 MHz, can also be generated to increment the counter by means of maintenance bit 11 of the Clock Status register. This operation should only occur, however, when the clock is disabled (ENA CT) and the rate selected is 1 MHz. Loading bit 11 of the Clock Status register generates a pulse at the beginning of the divide-by-10 counter chain, and that pulse can be used to verify proper operation of the clock counter.

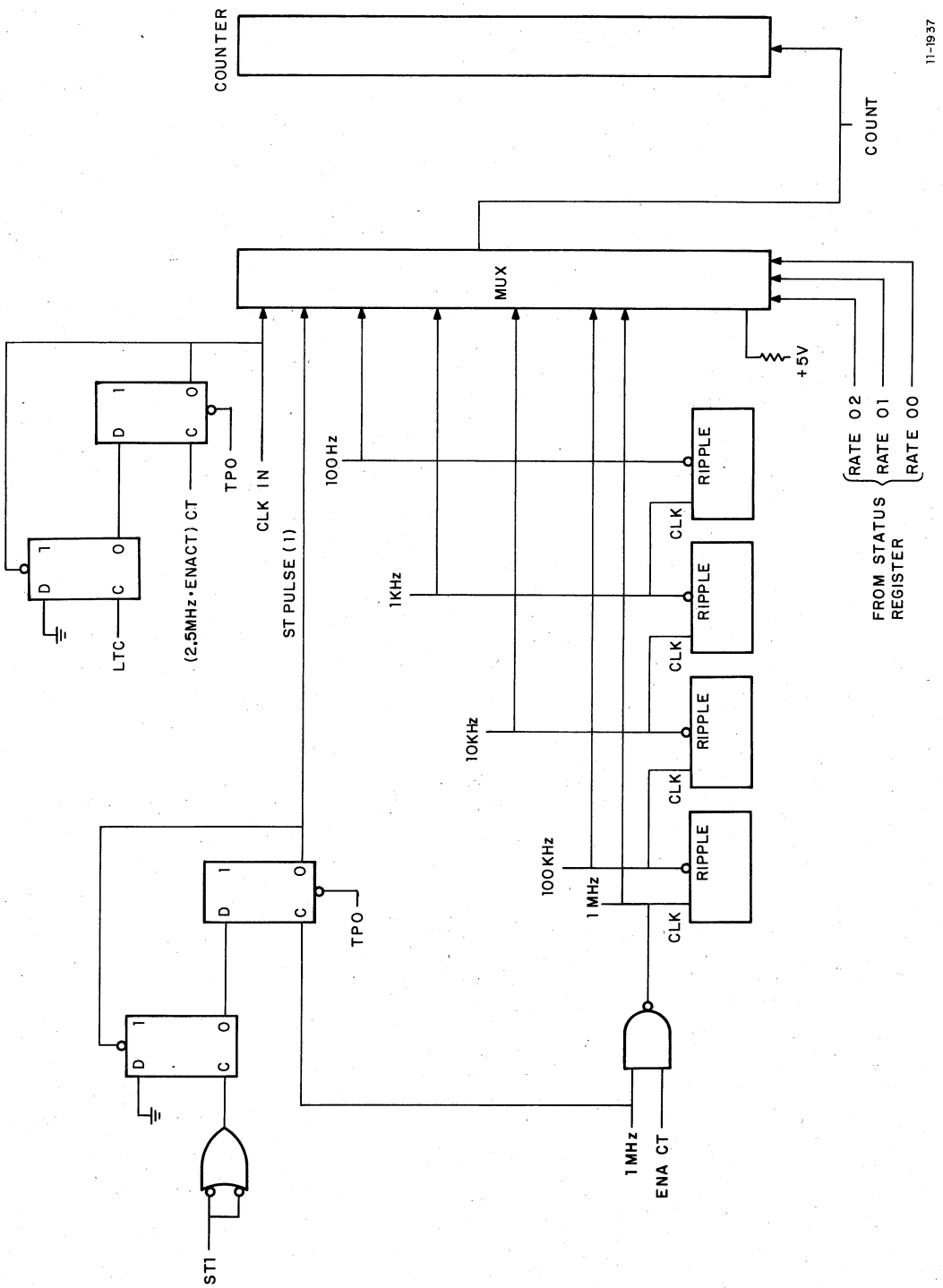

Figure 3-42 Rate Selection Logic

The line frequency input LTC (Figure 3-43), furnished by the power supply, clocks the LTC flip-flop and qualifies the CLK IN flip-flop. The output CLK IN immediately clears the LTC flip-flop and is applied to the multiplexer. The next TP0 clears the CLK IN flip-flop, and a complete count pulse is generated.

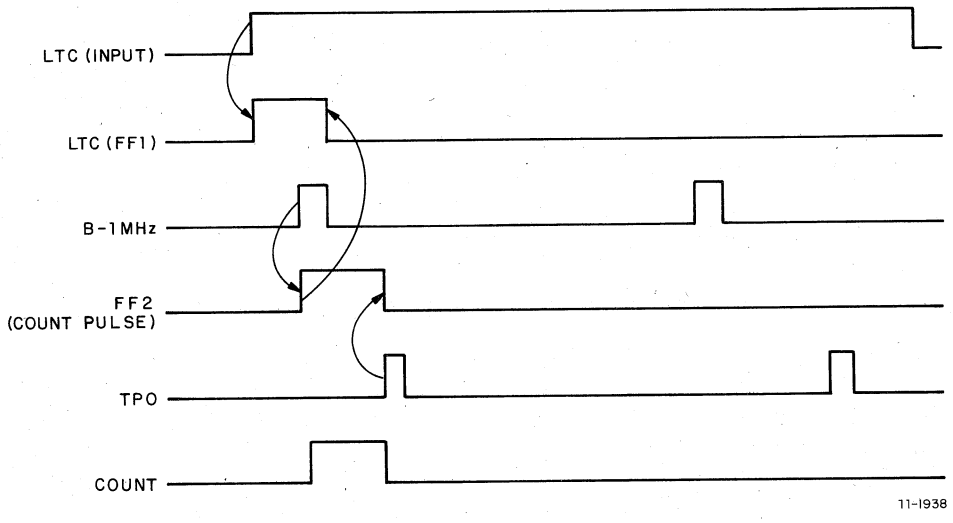

Figure 3-43 Count Pulse Timing Diagram

Schmitt trigger #1 is applied to a pulse-shaping network by way of a phone jack located on the front panel of the LPS11-S to produce the signal ST 1, which is synchronized with the 1 MHz clock to generate ST PULSE, and then ST PULSE is applied to the multiplexer also.

3.3.6 Interrupt and Flag Logic

When the clock requests an interrupt, the bus control gains control of the Unibus, vectors to the clock interrupt address, and notifies the clock when the interrupt is completed. Flag bits 15 and 07 of the Clock Status register denote which of two methods of interrupt is initiated.

The first method entails the use of Schmitt trigger #1. When an external signal is applied (Paragraph 3.3.5), the signal ST PULSE is generated (Figure 3-44), and is used to set bit 15 of the Status register. If the enable bit (bit 14 of the Status register) is qualified (INT ENA 2), the interrupt flip-flop INT REQ B is clocked. The output INT REQ B is sent to the bus control for processing. When the interrupt is complete, an INT DONE B signal is returned from the bus control to clear the INT REQ B flip-flop. Bit 15 of the Status register may be sampled at any time; however, the program must clear this bit.

The second method of initiating an interrupt is through the mode circuitry (Paragraph 3.3.7). At the completion of a mode operation, a pulse, either OV LD or CLBF→BF, is generated, setting a flag. An interrupt is generated if bit 06 of the Clock Status register (INT ENA 1) is qualified (Figure 3-45). The subsequent interrupt process is the same as that described above for the first method of initiating an interrupt. Completion of mode operations entails an overflow occurring or Schmitt trigger #2 firing.

If these two events occur simultaneously, only one interrupt occurs, and it is necessary to sample the flags of the Status register to identify the interrupt.

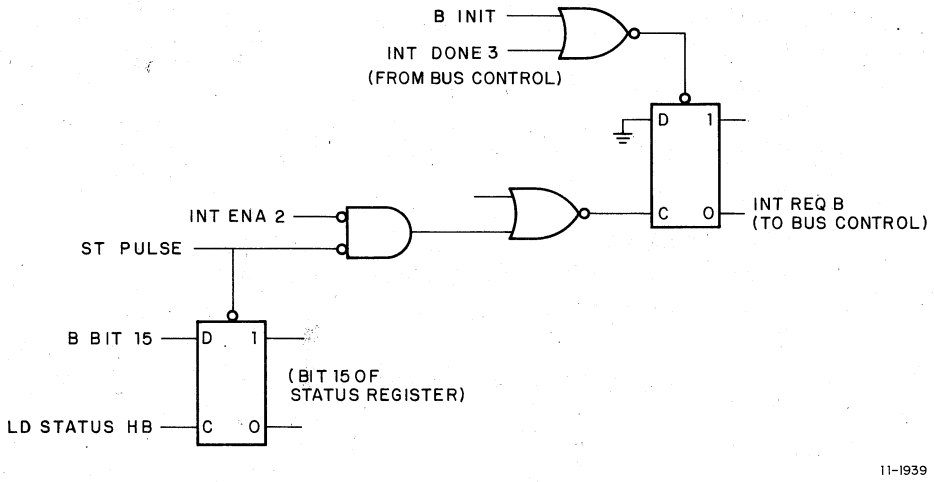

Figure 3-44 Schmitt Trigger #1 Interrupt Logic

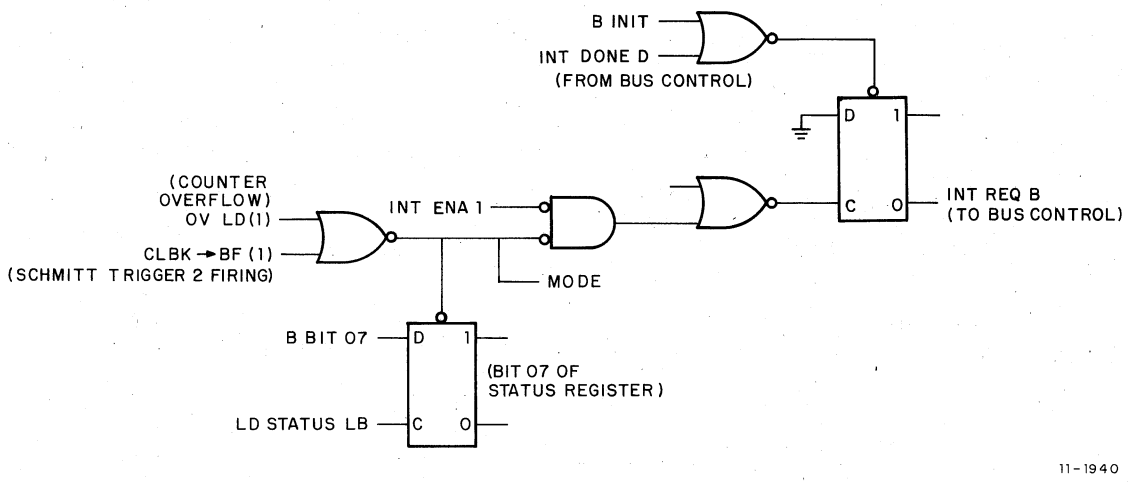

Figure 3-45 Mode Interrupt Logic

3.3.7 Mode Control

All clock counter and preset buffer transfers are controlled by the configuration of mode bits 09 and 08 of the Clock Status register, as discussed in Paragraph 3.3.2 and set forth in Table 3-15.

Table 3-15
Clock Status Register Bits 09 and 08

Mode of Operation	Clock Status Register	
	Bit 09*	Bit 08*
Mode 0	0	0
Mode 1	0	1
Mode 2	1	0
Mode 3	1	1

*Bit 09 generates signal MODE 01, bit 08 generates signal MODE 00.

3.3.7.1 Single Interval Mode (Mode 0) – During mode 0, the counter counts from a preset value at a preselected rate until it overflows, setting the Mode flag (bit 07 of the Clock Status register) and creating an interrupt (if enabled), stopping the counter, and reloading the counter with the preset value.

When the count in the clock counter makes the transition from 177777_8 to 000000, overflow pulse A OV is generated.

NOTE

A OV is hard-wired to B OV, which is applied to the A/D converter as one of the external starts (Paragraph 3.2.6), and can be monitored on the front panel.

The B OV pulse sets the overflow flip-flop to create OV LD (Figure 3-46). The B OV pulse occurs during the 1 MHz count state (Figure 3-47).

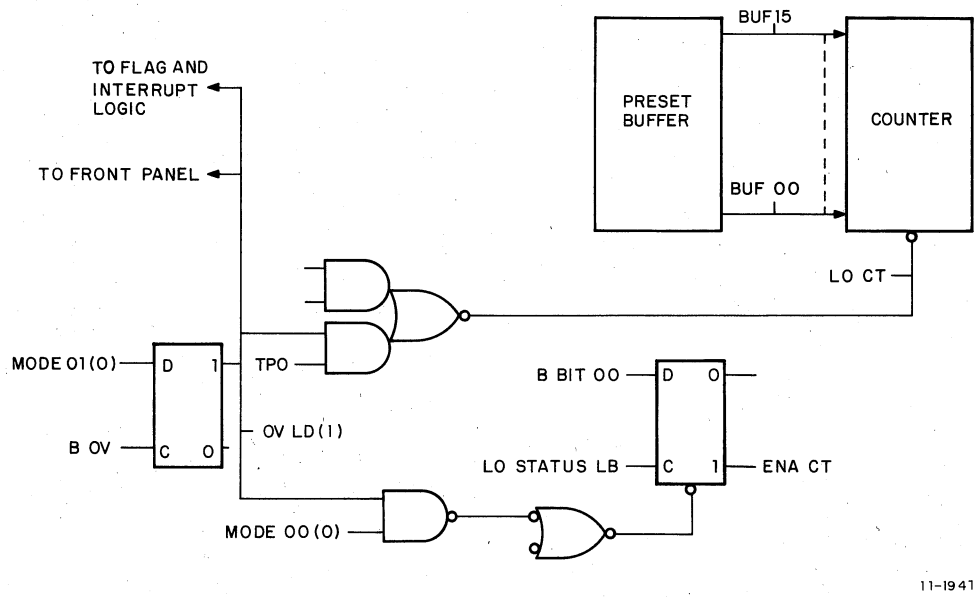

Figure 3-46 Mode 0 and 1 Logic

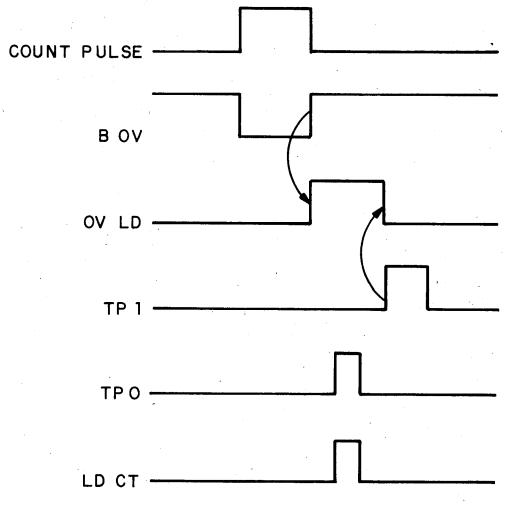

Figure 3-47 Overflow Timing Diagram

OV LD (1) is gated with Status register bit 08 to clear the enable count flip-flop (Status register bit 00), and the counter stops counting until it is reinitialized by the program. The signal OV LD (1) is inverted to become MODE, and simultaneously sets the Mode flag (Status register bit 07) and generates an interrupt if the interrupt is enabled (Status register bit 06). The OV LD signal is also gated with TP0 to create the LD CT (load counter) signal, which clocks the value in the Preset Buffer register into the clock counter, reinitializing the counter for the next experiment. The OV LD flip-flop is cleared 300 ns later by TP1. The value in the Preset Buffer register may be changed by loading a new value.

3.3.7.2 Repeated Interval Mode (Mode 1) – The mode 1 functions are similar to those of mode 0. The counter counts from a preset value at a selected rate until it overflows, setting the Mode flag, creating an interrupt if enabled, and reloading the counter with the preset value. When in mode 1, however, the counter is not disabled, and continues to count up (Figure 3-46), with signal MODE 00 inhibiting the OV LD pulse from clearing the counter enable bit (Status register bit 00). At each overflow, the value of the Preset Buffer register is transferred to the clock counter, overflowing at some set interval. If the Preset Buffer register is changed, the counter preset value will not change until the next overflow.

3.3.7.3 External Event Timing Mode (Mode 2) – Mode 2 requires interaction with Schmitt trigger #2 input. A pulse from that input transfers the contents of the clock counter to the preset buffer (while the counter continues to run), sets the Mode flag, and creates an interrupt if enabled.

Schmitt trigger #2 input is applied to a pulse-shaping network by way of a phone jack located on the front panel, producing the signal ST2. The firing of Schmitt trigger #2 synchronizes the signal ST2 with TP1 to set the CKBF flip-flop (Figures 3-48 and 3-49). The multiplexer (MUX) normally passes the internal bus to the preset buffer; however, when the CKBF flip-flop is qualified, the multiplexer passes the output of the clock counter to the preset buffer via the B BUF 15:00 lines. At time state 2 (TS2), a preset buffer signal is generated (LOAD BUF) and the clock counter data is transferred to the preset buffer. Also, when the CKBF flip-flop is set, its output (CKBF BF(1)) sets the Mode flag and creates an interrupt if enabled. The CKBF flip-flop is cleared by the B-1MHz signal, and the clock continues to count while waiting for another external stimulus.

3.3.7.4 External Event Timing from Zero (Mode 3) – Mode 3 performs a function identical to that of mode 2. However, at TP3 time the clock counter is cleared by CLEAR CT (Figure 3-49), which is inhibited in mode 2 by bit 08. After each external event, the clock counter is cleared, and starts again from a zero base.

3.3.8 Schmitt Trigger – Pulse Shaping

The Schmitt trigger pulse-shaping circuits for both channels is identical, as can be seen on sheet 4 of drawing D-CS-M7016-0-1. These circuits compare a differential input voltage against a firing threshold that is determined on the front panel by a potentiometer. Hysteresis is achieved by not permitting the circuit to retrigger at the same threshold. Figure 3-50 is an example of hysteresis.

The voltage, V, clocks the comparator, which initiates the logic. However, the comparator voltage will not retrigger until the voltage falls 0.4V below the input threshold V, ensuring that noise on the input signal will not clock the comparator.

The differential inputs from the front panel enter an emitter follower circuit, which acts as a high-impedance buffer, providing the 50 kΩ input impedance and protecting the inputs. The outputs of this buffer are applied to an operational amplifier that is used as a comparator to provide the hysteresis and slope determination of the Schmitt triggers.

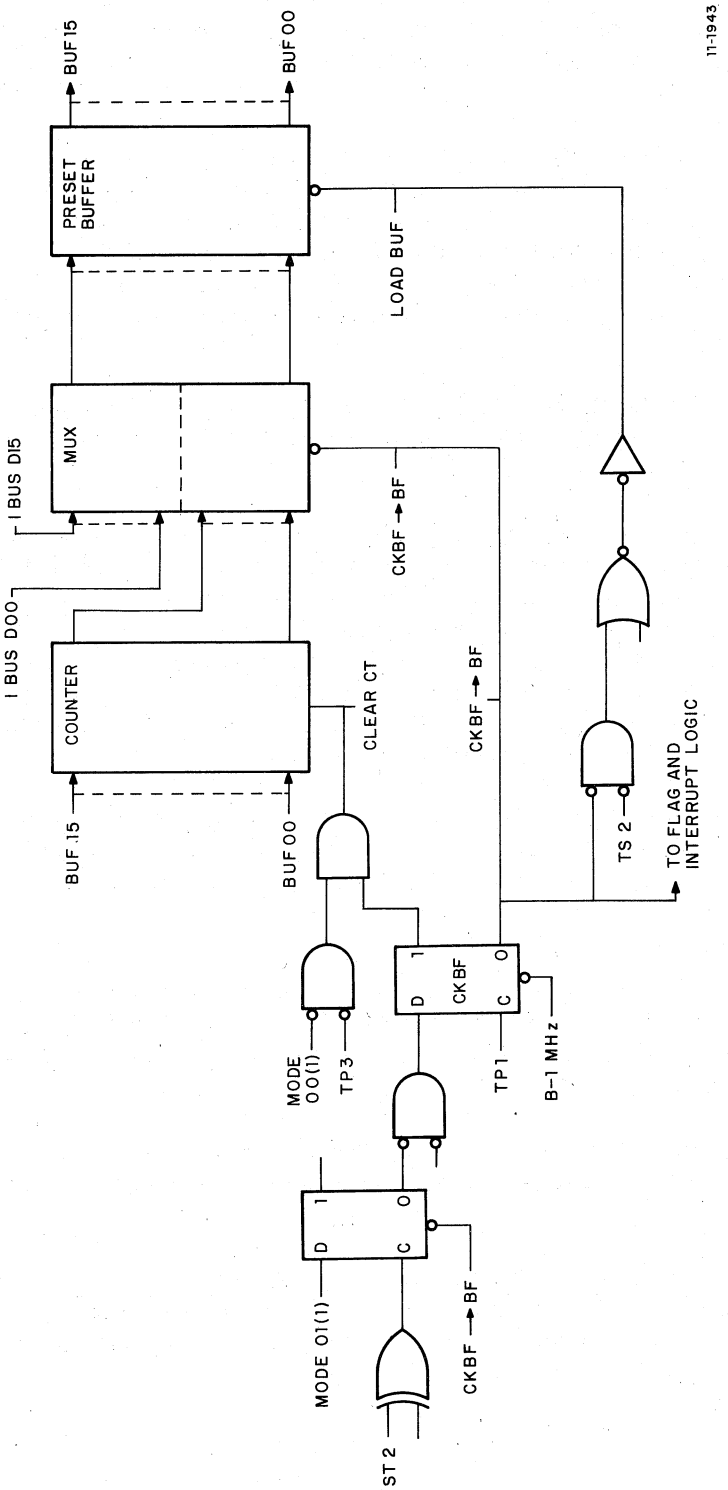

Figure 3-48 Mode 2 and 3 Logic

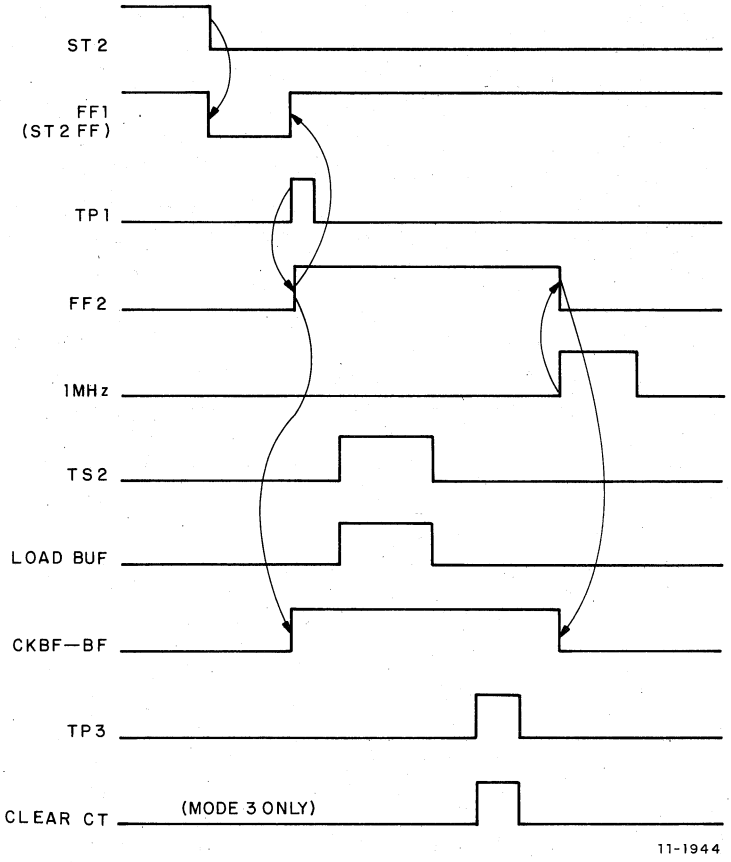

Figure 3-49 Mode 2 and 3 Timing

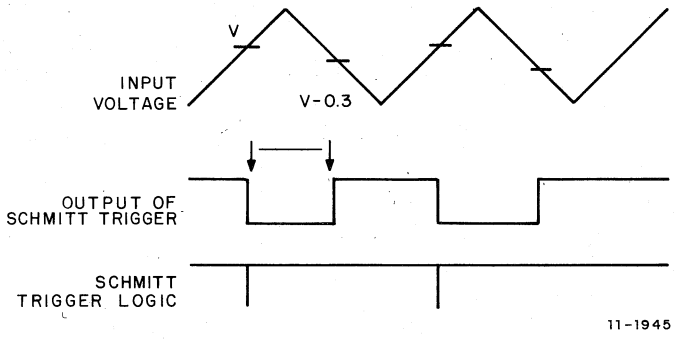

Figure 3-50 Hysteresis Example

If a ramp were to be injected into the Schmitt trigger circuitry (Tables 3-16 and 3-17 and Figure 3-51), which spans + and -2V, and the circuit were to fire at a 1V threshold on a positive-going slope, the initial voltages of the system at the -2V point would be as shown in column A of Table 3-16. As input voltage (V_{in}) increases, the differential voltage (V_D) across the operational amplifier starts positive. When V_{in} reaches 1V, the operational amplifier output voltage (V_{out}) changes from a negative to a positive voltage. This occurs because the differential voltage is zero and going positive, increasing the logic voltage (V_{log}) to 4V, which clocks the Schmitt trigger synchronizing circuit. At the same time, V_H switches from -0.2V to +0.2V due to the connection to V_{out} through R1. This change is reflected back on the differential voltage V_D, making it more positive and ensuring that no false triggering will occur. Only when the input voltage (V_{in}) drops 0.4V below 1V does the circuit retrigger, at which time the output voltage (V_{out}) swings negative, forcing the logic voltage (V_{log}) to -0.7V and returning the hysteresis voltage (V_H) to -0.2V. This -0.4V change is reflected back to the differential voltage, pulling it more negative. Table 3-17 shows five points on an input voltage swing and gives the voltages at various points of the circuitry.

Table 3-16
=1 Voltage Threshold Positive Slope Chart

	A	B	C	D	E
$V_{in} = V_A - V_D$	-2	+1	+2	+.6	-2
V_A	-2	+1	+2	+.6	-2
V_B	0	0	0	0	0
V_{pot} (Threshold)	+.8	+.8	+.8	+.8	+.8
V_H (Hysteresis)	-.2	-.2 / +.2	+.2	+.2 / -.2	-.2
$V+ = \left(\frac{V_A - V_H}{2}\right) + V_H$	-1.1	+.4 / .6	+1.10	+.4 / +.2	-1.1
$V- = \left(\frac{V_B - V_{pot}}{2}\right) + V_{pot}$	+.4	+.4	+.4	+.4	+.4
$V_D = V+ - V-$	-1.5	0 / +.2	+.7	0 / -.2	-1.5
V_{out}	-12.5	-12.5 / +12.5	+12.5	+12.5 / -12.5	-12.5
V_{log}	-.7	-.7 / +4	+4	+4 / -.7	-.7
Changes Due to V_{out} Changing					
V_H	- - -	+.4	- - -	-.4	- - -
V+	- - -	+.2	- - -	-.2	- - -
V_D	- - -	+.2	- - -	-.2	- - -

Table 3-17
=1 Voltage Threshold Negative Slope Chart

	F	G	H	I	J
$V_{in} = V_A - V_D$	+2	+1	−2	+1.4	+2
V_A	+2	+1	−2	+1.4	+2
V_B	0	0	0	0	0
V_{pot} (Threshold inverted)	−1.2	−1.2	−1.2	−1.2	−1.2
V_H	−.2	−.2 / +.2	+.2	+.2 / −.2	−.2
$V+ = \left(\frac{V_B - V_H}{2}\right) + V_H$	−.1	−.1 / +.1	+.1	+.1 / −.1	−.1
$V- = \left(\frac{V_A - V_{pot}}{2}\right) + V_{pot}$	+.4	−.1	−1.6	+.1	−.1
$V_D = V+ - V-$	−.5	0 / +.2	+1.6	0 / −.2	−.5
V_{out}	−12.5	−12.5 / +12.5	12.5	+12.5 / −12.5	−12.5
V_{log}	−.7	−.7 / +4	+4	+4 / −.7	−.7
Changes Due to V_{out} Changing					
V_H	— — —	.4	— — —	−.4	— — —
V+	— — —	+.2	— — —	−.2	— — —
V_D	— — —	+.2	— — —	−.2	— — —

To fire on a negative slope (Figure 3-51), the polarity of the potentiometer voltage (threshold–V_{pot}) and the differential input voltage (V_{in}) must be reversed, making the operation identical to a positive slope function, except that retriggering occurs at 1.4V because of the slope being reversed.

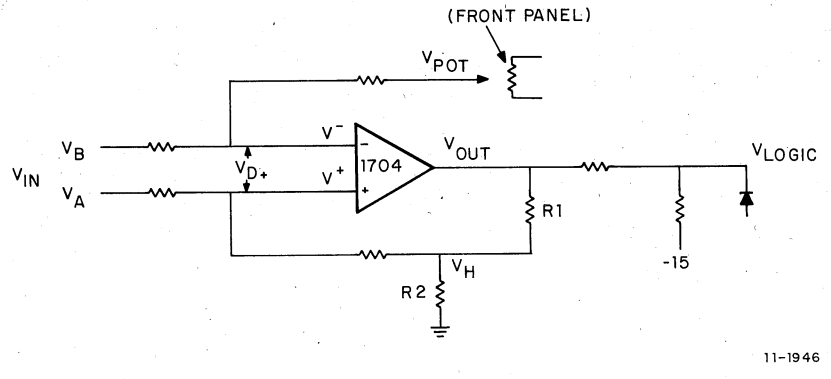

Figure 3-51 Schmitt Trigger Simplified Schematic Diagram

Two jumper wires on the Schmitt trigger circuitry permit increasing the hysteresis voltage from 0.4V to 2V. The hysteresis voltage (V_H) is determined by the voltage divider network of R1 and R2.

3.4 LPSVC DISPLAY CONTROL

The LPSVC display control provides X and Y coordinates to either an external X-Y recorder or a visual display to position a graphic data point. The position of the data point is determined by converting digital data to equivalent analog voltages, which, when developed, generate a pulse to intensify the data points.

The LPSVC display control is primarily used with DEC's VR14 or VR20 display, but can also be used with any Tektronix 604, 602, RM503, 611, 613 (storage scope), or equivalent oscilloscope. The LPSVC can also be used to run external digital-to-analog converters.

3.4.1 Block Diagram Discussion

The block diagram in Figure 3-52 illustrates the relationship between the LPSVC display control, the bus control, and the processor Unibus.

The bus control decodes the display control address, and processes all of the input/output control signals between the display control and the Unibus. Paragraph 3.1 contains a detailed description of the operation of the bus control.

The LPSVC display control option consists of two modules, the display controller module and the D/A module. The display controller module (M7019) comprises a Status register, a mode control, a register control, an interrupt and flag control, and a delay and intensifier circuit (refer to drawing D-CS-M7019-0-1, sheets 1 through 3).

The Status register is a read/write byte-operable register with a program-controlled bit content that determines the operation of the display control circuits and the appropriate external recorder and display unit functions.

Four modes of operation can be implemented by the mode control circuits. In mode 0, a point may be displayed via the intensification bit. Mode 1 displays when the X axis register is loaded, mode 2 displays when the Y register is loaded, and mode 3 displays when either the X or the Y register is loaded.

The register control circuit decodes a portion of the Status register output to select the digital-to-analog converter and control X, Y, or external digital-to-analog converter loading operations.

The interrupt and flag control circuits produce an interrupt output to the central processor via the bus control.

The delay and intensification circuit shapes and delays the intensification pulse output to allow the display to settle before application of the intensification pulse. This delay will vary depending upon the type of display used, and can be adjusted by means of jumpers.

Conversion of digital signals to analog voltages for recording or display purposes is accomplished by the X and Y registers and corresponding digital-to-analog converters. These circuits are located on the D/A module (A625). Control of these functions as well as internal timing and certain external recorder and display unit functions are affected by the display controller module.

3.4.2 Programming

The LPSVC display control is programmed through the Status register and the X and Y registers. The Status register is a read/write byte-operable register. Figure 3-53 illustrates the Status register bit assignments, and Table 3-18 provides a brief functional description of each.

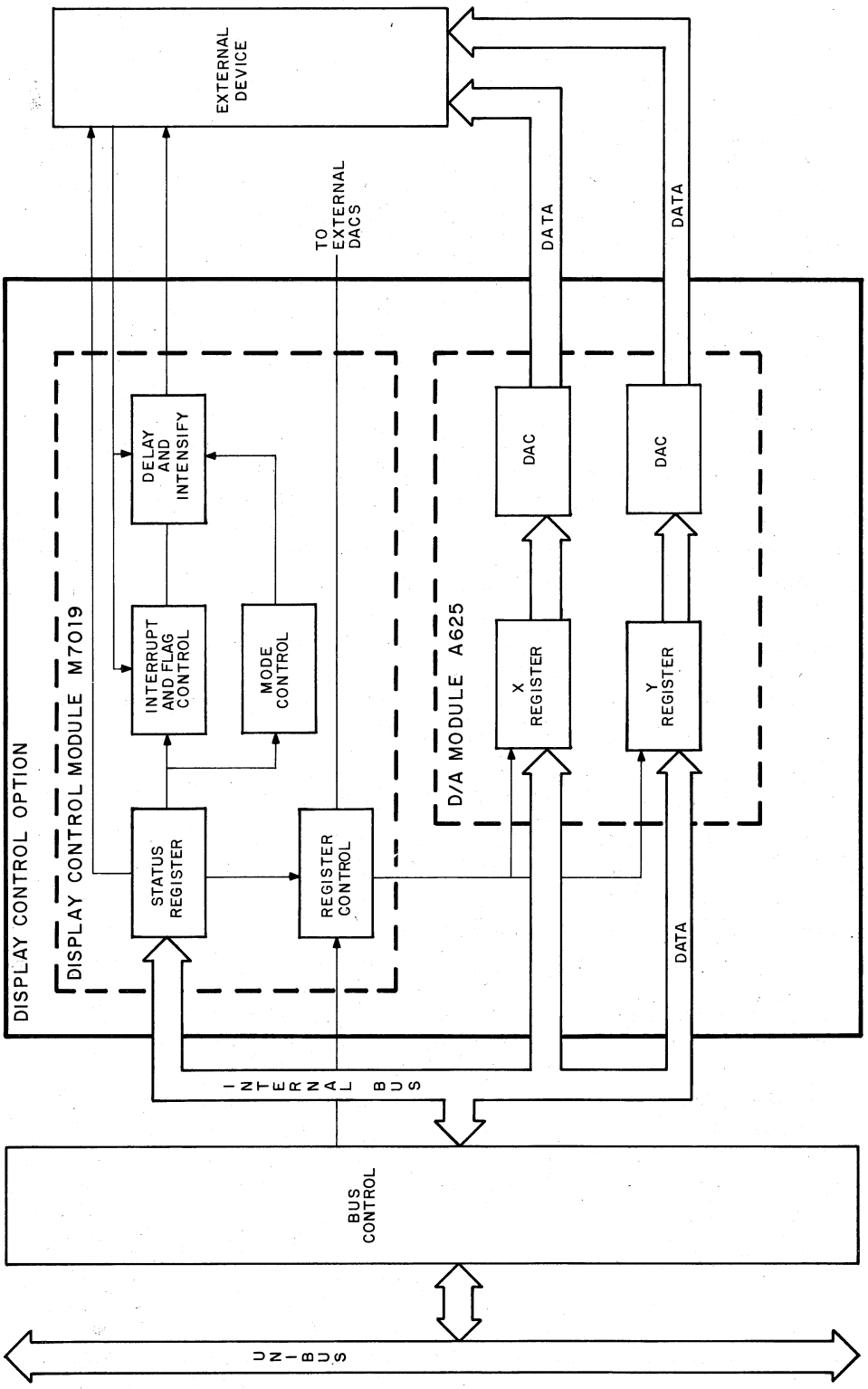

Figure 3-52 Display Control Block Diagram

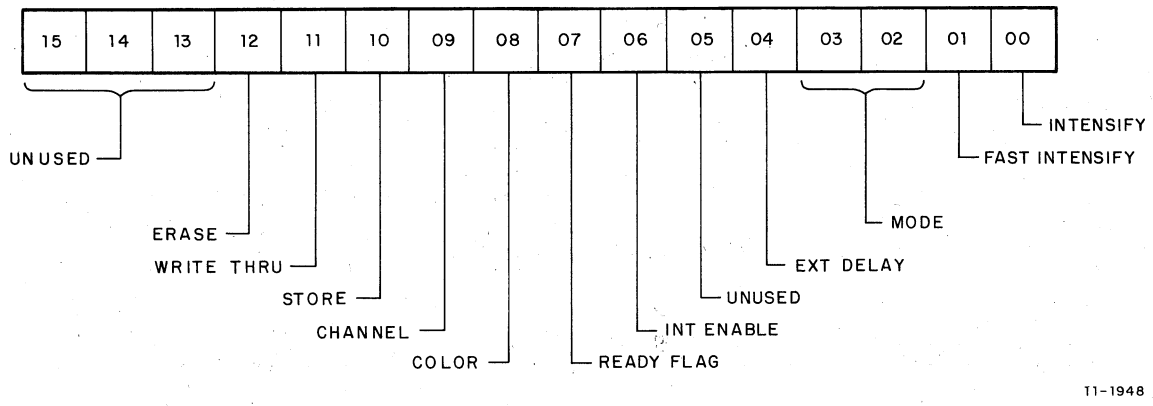

Figure 3-53 Display Control Status Register Bit Assignments

Table 3-18
Display Control Status Register Bit Functions

Bit	Name	Function
15–13	Unused	Always reads 0
12	Erase (Write Only)	Bit 12 = 1, erase data in the store scope (write only).
11	Write Thru (Read/Write)	Bit 11 = 1, an intensified point, will not be stored even though the user is in the store operation.
10	Store (Read/Write)	Bit 10 = 1, all intensified points will be stored.
9	Channel (Read/Write)	Bit 9 = 0, channel 1 Bit 9 = 1, channel 2
8	Color (Read/Write)	Bit 8 = 0, green mode Bit 8 = 1, red mode
7	Ready Flag (Read Only)	Bit 7 = 0, the scope is not ready; do not load or intensify points. Bit 7 = 1, the scope is ready.
6	Interrupt Enable (Read/Write)	Bit 6 = 1 and bit 7 in transition from a 0 to a 1 will cause an interrupt.
5	Unused	Always reads 0
4	EXT Delay (Read/Write)	When bit 4 = 1, all internal timing stops. When the external device (scope or X-Y recorder) returns a DONE signal, an intensify pulse will be generated and the Ready flag will be set.

Table 3-18 (Cont)
Display Control Status Register Bit Functions

Bit	Name	Meaning and Operation
3,2	Mode (Read/Write) Normal X Mode Y Mode XY Mode	03 02 0 0 Intensification with bit 0 only 0 1 Intensification on loading X register 1 0 Intensification on loading Y register 1 1 Intensification on loading X or Y
1	Fast Intensify Enable (Read/Write)	Bit 1 = 0, all scope settling delays are as defined for each scope. Bit 1 = 1, all scope settling delays are 3 μs.
0	Intensify (Write Only)	Bit 0 = 1, any coordinate in X and Y register will be intensified (write only).

When the LPSVC is used in conjunction with a scope, a scope grid coordinate scheme similar to that shown in Figure 3-54 is used. The control display takes the form of a 4096_{10} X 4096_{10} dot array. Under program control, a point may be displayed momentarily at any point in this array.

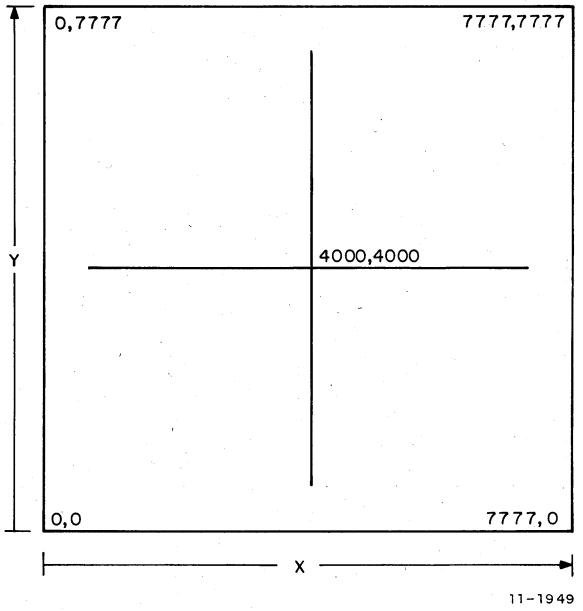

Figure 3-54 Display Control Grid Coordinate Scheme

The X and Y registers are read/write registers, but are not byte-oriented. Figure 3-55 illustrates their bit assignments.

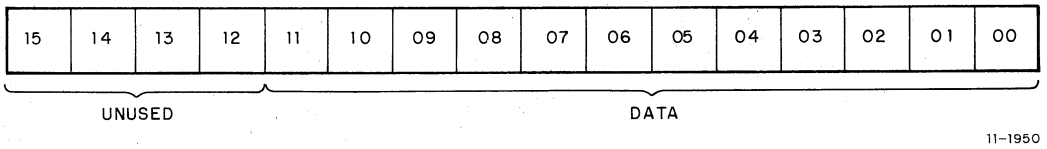

Figure 3-55 X and Y Register Bit Assignments

3.4.3 Status Register Gating

The bus control transmits four decoded address select lines (SELECT 7, 8, 9, and 10) and input/output control signals to the display control. SELECT 7 is used to address the Status register (drawing D-CS-M7019-0-1, sheet 2). When gated with the OUT signals, SELECT 7 generates the load commands that permit byte-oriented data from the central processor to be loaded. When SELECT 7 is gated with the IN signal, a read command is generated, permitting data from the Status register to be gated to the Unibus via the internal bus.

SELECT 7 generates I BUS RT ENABLE to be used by the bus control to permit a proper master-slave relationship. If the LPSVC option is not installed, the processor will time out and trap when using the Status register address.

The SELECT 8 and 9 lines are discussed in Paragraph 3.4.4. SELECT 10 deals with the EXT DAC section.

3.4.4 Intensification Modes

To display a point on the scope, an intensification pulse must be generated. The position of the displayed point depends on the contents of the X and Y registers, which are applied to a digital-to-analog converter to develop two coordinates, respectively. The point, which is displayed for the duration of the intensification pulse, can be generated by four different modes, controlled by Status register bits 02 and 03. Table 3-19 provides a brief description of each mode.

Table 3-19
Modes of Intensification

Status Register		Mode	Mode Function
Bit 03	Bit 02		
0	0	Normal	Intensification with bit 0 only
0	1	X Mode	Intensification on loading X register
1	0	Y Mode	Intensification on loading Y register
1	1	XY Mode	Intensification on loading X or Y

3.4.4.1 Normal Mode – During the normal mode of intensification, the intensify pulse circuitry is initiated (signal ST DEL) by loading the Status register with bit 00 = 1 (Figure 3-56).

NOTE
The other bit configurations in the Status register must be loaded at the same time.

The position of the point is determined by the contents of the X and Y registers. By addressing the X and Y registers, the contents of these registers can be changed while in the normal mode, without displaying a point.

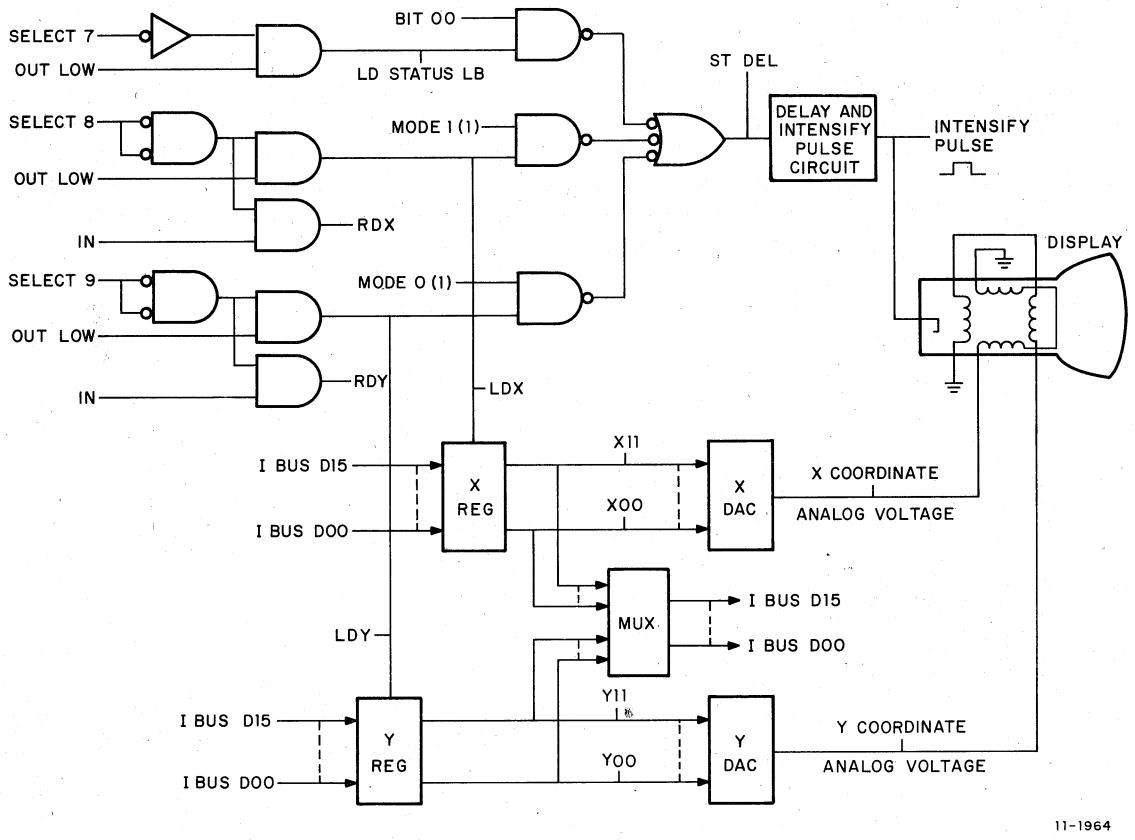

Figure 3-56 Modes of Intensifying a Point

3.4.4.2 X Mode – The intensify pulse can be initiated at the same time that the X register is loaded, with Status register bit 03 = 0 and bit 02 = 1. When the X register is addressed, SELECT 8 is ANDed with OUT LOW to generate LD X, which is the load pulse for the X register, and is simultaneously ANDed with mode 0 (Status register bit 02) to generate ST DEL, which triggers the intensify pulse circuitry.

This mode is useful when the X coordinate is changing while the Y coordinate remains constant.

3.4.4.3 Y Mode – The intensify pulse can also be initiated at the same time that the Y register is loaded, with Status register bit 03 = 1 and bit 02 = 0. When the Y register is addressed, SELECT 9 is ANDed with OUT LOW to generate LD Y, the load pulse for the Y register, and is simultaneously ANDed with mode 1 (Status register bit 03) to generate ST DEL, which triggers the intensify pulse circuit.

This mode is useful when the Y coordinate is changing while the X coordinate remains constant.

3.4.4.4 XY Mode – The XY mode is an ORing function of the two previously discussed X and Y modes. When either the X register or the Y register is loaded, an intensify pulse is initiated.

3.4.5 Deflection Delay Circuitry

3.4.5.1 Normal Delay – Because all oscilloscopes have a deflection settling time, the analog data (X and Y coordinates) applied to the oscilloscope must be delayed prior to intensification. The delay is determined by the delay control circuit (drawing D-CS-M7019-0-1, sheet 3). When intensification is requested and operation is not in the fast intensification mode (Status register bit 1 = 0), the first one-shot multivibrator is triggered (Figure 3-57). The trailing edge of the first one-shot triggers the 3 μs one-shot multivibrator. The combination of these two pulses determines the delay necessary to establish the correct deflection settling time.

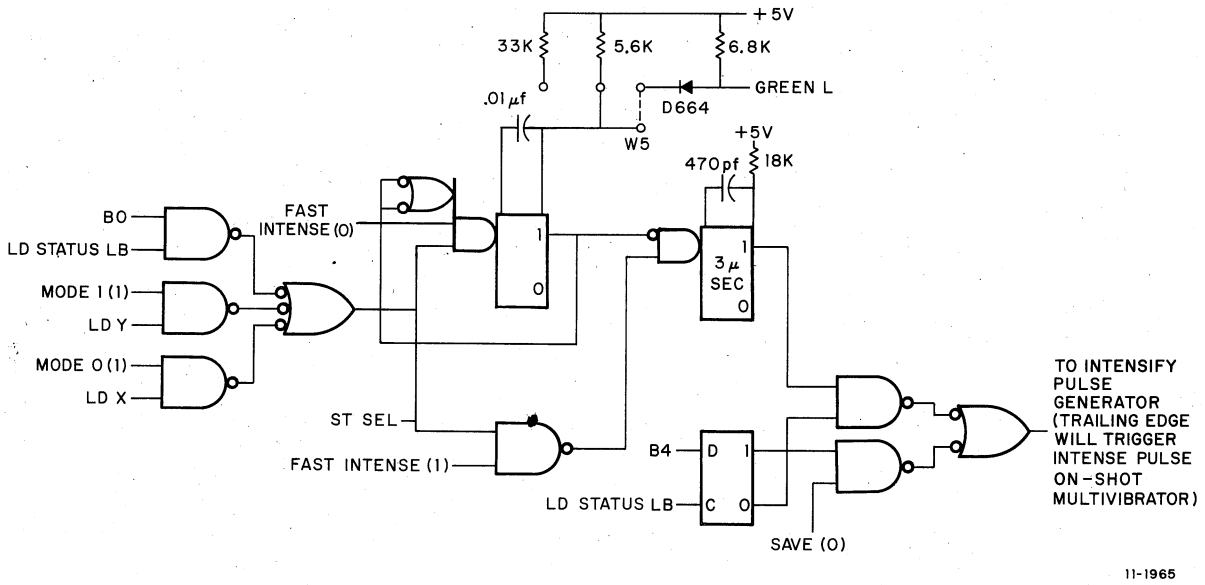

Figure 3-57 Deflection Delay Circuit

3.4.5.2 Fast Intensify – Status register bit 1 permits the user to bypass the first one-shot multivibrator, thus confining the scope settling delay to 3 μs. This is accomplished by inhibiting the input to the first one-shot multivibrator and enabling the trigger input to the 3 μs one-shot multivibrator. The fast intensify enable bit must not be loaded simultaneously with the intensify bit (bit 0).

3.4.6 VR20 Color Modes

3.4.6.1 Changing Modes (VR20 Setup Delay) – The DEC VR20 color display is capable of changing color modes from red to green, or vice versa, controlled by Status register bit 08. The VR20 normally operates in the green mode. When its circuitry is called upon to switch internal voltages to permit red mode operation, a delay is necessary, during which intensification cannot occur.

When Status register bit 08 sets, initiating a color mode change from green to red, the RED DELAY one-shot multivibrator (approximately 300 μs) is triggered (Figure 3-58). The trailing edge of RED DELAY clocks the DONE and SAVE flip-flops and generates an interrupt if the interrupt is enabled (Status register bit 06). Setting of the DONE flip-flop (Status register bit 07) or the occurrence of an interrupt indicate to the processor that the VR20 is ready to display data. The DONE flag is cleared by the COL PULSE one-shot multivibrator and the INT flip-flop is cleared by the completion of the interrupt (INT DONE E) (drawing D-CS-M7019-0-1, sheet 3).

When Status register bit 08 is cleared, initiating a color mode change from red to green, the operation is similar except that it is the GREEN DELAY one-shot multivibrator (approximately 1.6 ms) that is triggered rather than the RED DELAY.

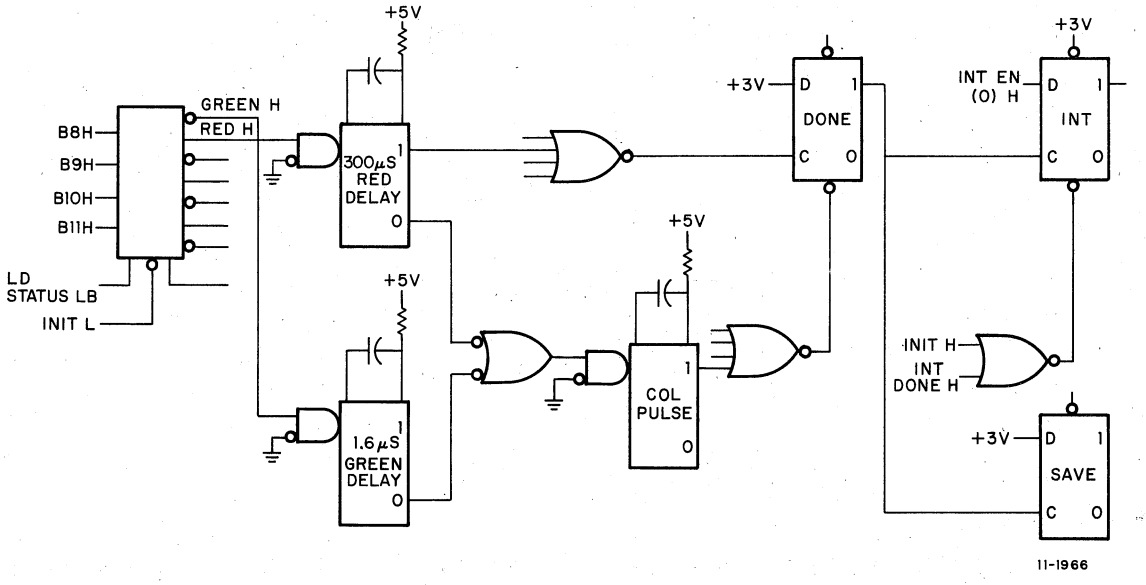

Figure 3-58 Delay Circuitry for VR20 Setup Time

3.4.6.2 Green Mode – The deflection delay pulse allows the deflection circuitry time to settle before intensifying the point. In the green mode, the delay time is approximately 21 μs.

The signal GREEN L reverse biases the D664 diode on the first delay, permitting only the 5.6K resistor and the .01 μF capacitor to form the RC network shown in Figure 3-59. The resultant 18 μs delay, together with a 3 μs one-shot, accounts for the total deflection settling time of 21 μs.

The intensify pulse is used to intensify the point on the scope. In the green mode, the intensify pulse is approximately 1 μs. The signal DELAY H forward biases the D664 diode on the INTEN PULSE one-shot multivibrator, placing the 39K and 5.6K resistors in parallel to form the RC network.

3.4.6.3 Red Mode – In the red mode, the delay time necessary to allow the scope deflection circuitry to settle is only 15 μs. When the signal GREEN L is disqualified (Figure 3-57), the D664 is forward biased, putting the 6.8K resistor in parallel with the 5.6K resistor, decreasing the total resistance of the RC network, and decreasing the delay time from 18 μs to 15 μs.

The red mode requires an intensify pulse of 6 μs, compared to 1 μs for the green mode. In the red mode, the signal DELAY H is disqualified (Figure 3-59), reverse biasing the D664 diode and removing the 5.6K resistor from the parallel RC network, which then consists of a 39K resistor and 470 pF capacitor. The resultant delay is 6 μs.

3.4.7 VR14-VR20 Channel Selection

The VR14 and VR20 scopes are each capable of displaying data on two channels. Status register bit 09 is the channel selection bit, and is sent directly to the scope.

3.4.8 Storage Scope Circuit

Storage scopes normally have two modes of operation, store and nonstore. Status register bits 10, 11, and 12 are all associated with the operation of the storage scope.

In the nonstore mode (bit 10 = 0), the scope displays points but does not store points. The deflection settling delay depends on the W5 jumper installed (Figure 3-57). The width of the intensify pulse is 1 μs.

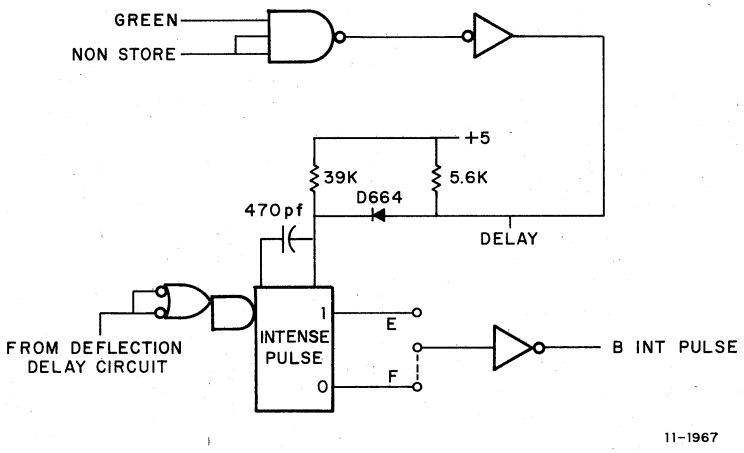

Figure 3-59 Intensify Pulse Generator

In the store mode (bit 10 = 1), the intensify pulse is increased to 6 μs. The signal DELAY is disqualified, so that only the 39K resistor and the 470 pF capacitor form the RC network, In this mode, the scope circuitry stores and continuously refreshes the intensified points until the LPS11-S display control orders them erased.

To erase the stored display, the signal ERASE (Status register bit 12 = 1) is applied to the storage scope, which enters the erase cycle and grounds the signal ERASE RETURN, clearing Status register bit 12. ERASE RETURN remains grounded during the entire storage scope erase cycle. When that cycle is completed, ERASE RETURN returns high, clocking the DONE flag and the SAVE flip-flop and creating an interrupt, if enabled. Figure 3-60 illustrates storage scope logic.

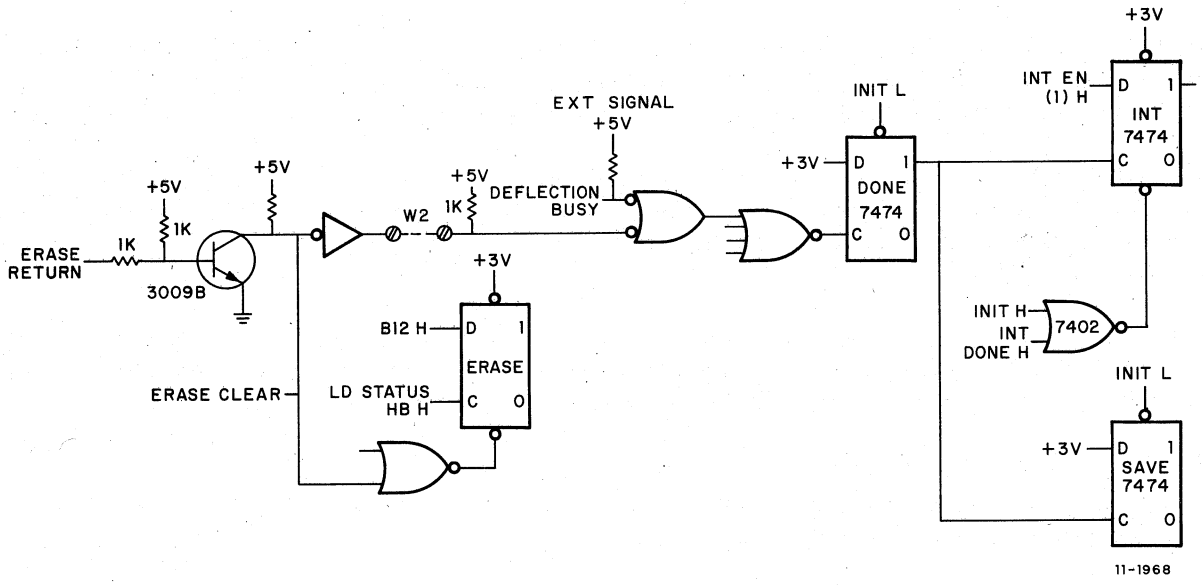

Figure 3-60 Storage Scope Logic

3.4.9 Flag and Interrupt Circuits

Upon completion of any display operation entailing internal or external delays, the DONE flag (Status register bit 07) goes true. If the interrupt enable (Status register bit 06) is set, the positive transition of the flag bit clocks the interrupt flip-flop.

There are four ways in which the DONE (ready for next operation) flag can be set. The first way is during the intensification of a point, when the ST DEL signal clears the flip-flop and, at the completion of the delay cycle, the intensify pulse clocks the DONE flag.

The second method is initiated by changing the VR20 color bit (Status register bit 08), generating a time pulse (COLOR PL), which clears the DONE flag.

The third method occurs when an erase command is initiated, and the output of the ERASE flip-flop clears the DONE flag. When the external scope erase delay times out, an ERASE RETURN signal is returned to the display control, resetting the DONE flag.

The fourth method occurs when the external scope is allowed to determine the deflection delay time internally. The signal ST DEL clears the DONE flag; at the completion of the external scope operation, the signal DEFLECTION BUSY resets the DONE flag.

3.4.10 A625 Digital-to-Analog Converter

The digital-to-analog converter (DAC) comprises two 12-bit latching registers and two digital-to-analog converter circuits (drawing D-CS-A625-0-1). The DAC converts a 12-bit digital value into an analog voltage for use by an external X-Y recorder or visual display. The analog voltage ranges from ±1/2V, ±5V, ±10V, 0–1V, or 0–10V, depending upon the jumper arrangement of the A625 module.

Data from I BUS D11:D00 is loaded into the X or Y registers upon receipt of signals LD X or LD Y from the scope control board. Signal INIT L is used to clear the registers. The register output is applied to the two corresponding X and Y 12-bit DACs (A6000s), which convert the digital input into representative analog voltages. The X and Y converters are identical, so that a discussion of the X DAC would also apply to the Y DAC.

Any change of data in the X register is immediately converted by amplifier E2, which is a fast-settling operational amplifier. Amplifier E1 is a current booster that enables the output to drive capacitive loads, such as a scope cable.

The amplifier gain and the range of the analog output are determined by the module jumper configuration. Resistance Rx (refer to Note 1 on sheet 2 of drawing D-CS-A625-0-1) is established by inserting the proper split lug jumper on the module. For example, to obtain a 0–10V output range, jumpers W8, W9, and W11 are inserted. Insertion of jumper W11 grounds the offset voltage to achieve unipolar outputs. Jumpers W8 and W9 alter the circuit gain as shown in Figure 3-61.

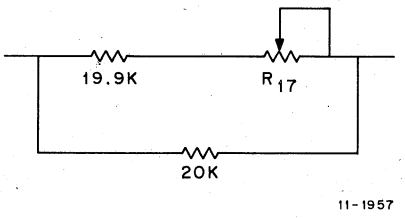

Figure 3-61 Example of Rx Value

The 20K and 19.9K resistors are located within the (A6000) DAC. When the gain potentiometer is properly adjusted, Rx will appear as a 10K resistor. The 0–1 mA current source applied to two parallel 2K resistors results in a 0–1V digital-to-analog converter output.

Adding the -1V offset to achieve a bipolar output results in adding a -1/2V shift to the voltage input, due to the voltage division between the 2K resistors in the DAC. The resulting output will be bipolar ±5V.

Note 1 on drawing D-CS-A625-0-1, sheet 2, shows the effect of different jumper arrangements.

The balance potentiometer R15 is used to adjust the output voltage to midscale when a 4000 code is entered into the X input register. Diodes D7 and D8 limit the output excursion to ±6.3V when jumper W12 is installed. This jumper must always be installed when the output range does not exceed ±6.3V to protect scopes from overdrive in the event of a system failure.

3.4.11 Intensify Circuit

The output of the delay intensification circuit is applied to the intensification one-shot multivibrator and generates a pulse, depending upon the polarity required (as determined by jumpers E and F), which is applied to inverter E13. The output of E13 is applied to the base of transistor Q6, which provides drive for the complementary-symmetry power-amplifier stage, consisting of Q7 and Q8.

Transistor Q6 may be in either a saturated or a cut-off state. In a saturated state, with jumper D or W1 installed, Q6 provides +4V drive to the junction of R54 and jumpers W3, A, B, and C. In a cut-off state, with neither D nor W1 installed, Q6 provides 0.7V drive.

The power amplifier stage (Q7, Q8) provides the current necessary to drive long cables. Jumpers W3, A, B, and C permit selectable bias for this stage.

3.5 DIGITAL I/O – LPSDR-A

The LPSDR-A digital I/O option permits 16 bits of data to be transferred between the LPS11-S and an external device. Drawings D-CS-M7023-0-0 sheets 1A through 4 of the Engineering Drawings illustrate the logic for the LPSDR-A.

3.5.1 Block Diagram Description

The LPSDR-A option (Figure 3-62) comprises a read/write output register, input register, status register, interrupt control, and two relays. The bus control, described in Paragraph 3.1, decodes the I/O address and processes all bus control signals. Because of this feature, the LPSDR-A may only be used with the LPS11-S.

When data is transferred to the input register from an external device, one of three modes (Stimulus, Word Transfer, and Mix) may be utilized (jumper and switch selectable).

When data is to be transferred from the Unibus to an external device, the 16-bit buffered output register is addressed under program control.

The status register contains two flags (one for input and one for output), two interrupt enable bits, two relay control bits, and two maintenance bits. All input and output operations are controlled by the status register.

There are two interrupts associated with the LPSDR-A which when enabled, indicate that data has been loaded into the input buffer (INT C) and that data has been accepted by the external device (INT D).

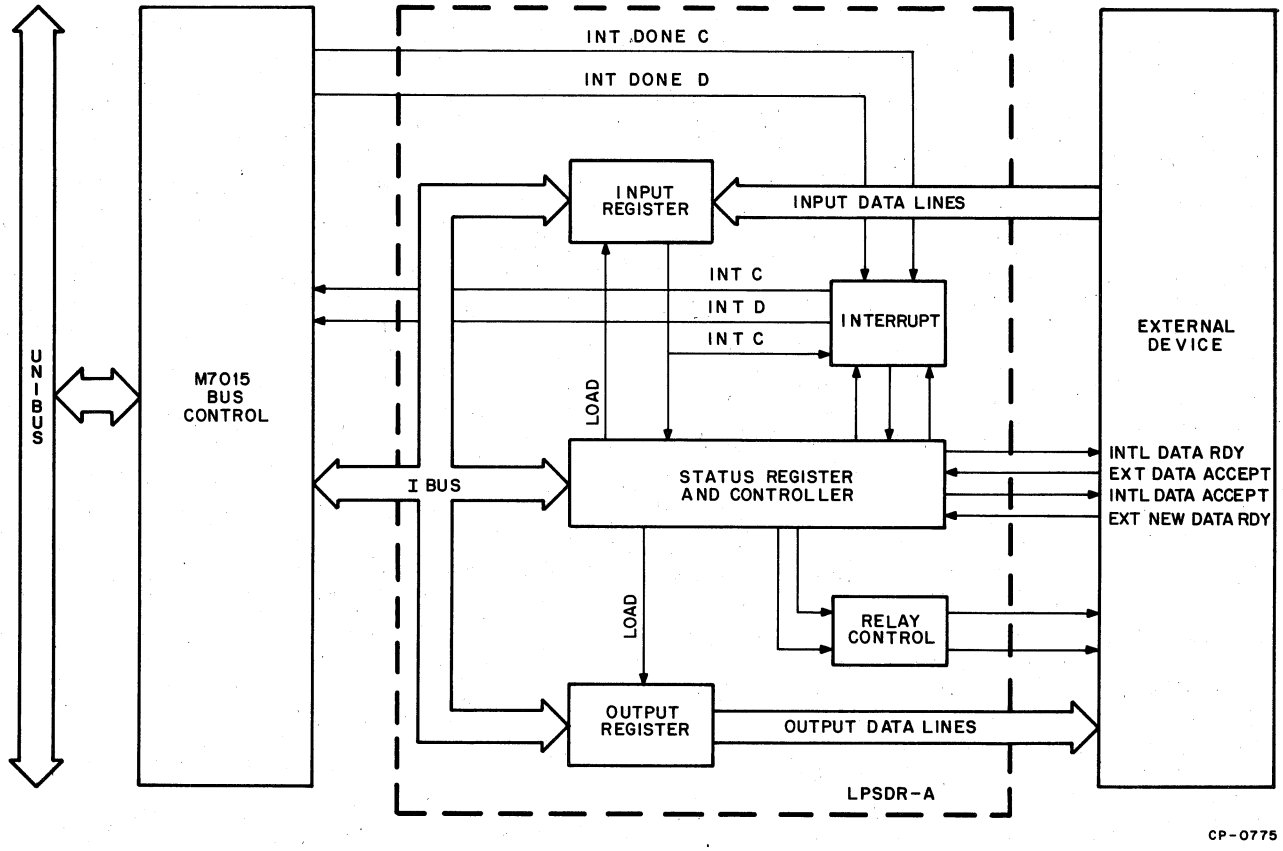

Figure 3-62 Digital I/O Block Diagram

3.5.2 Register Addressing

The bus control transmits three decoded address control signals (SELECT 4, 5, 6) plus input/output control signals.

The SELECT 4 signal is used to address the status register (Figure 3-63) during a read/write operation. In the read operation, SELECT 4 is gated with the IN signal to generate the RD STATUS signal (Figure 3-64). The contents of the status register are then placed on the bus. During a write operation, SELECT 4 is gated with OUT HIGH or OUT LOW to generate the appropriate LD STATUS HIGH or LD STATUS LOW signal to load data from the bus into the status register.

Basically the input and output registers operate in the same manner as the status register in response to the signals SELECT 5 and SELECT 6 respectively. The SELECT 5 signal gates the contents of the input register (external data) onto the internal bus by generating the READ INPUT signal. SELECT 5 also gates with OUT HIGH and OUT LOW to load the input register, thereby clearing the bit set. The SELECT 6 signal is gated with OUT HIGH and/or OUT LOW to transfer the bus data to an external device via an LD OUT LOW or LD OUT HIGH signal. SELECT 6 also gates with IN to transfer the contents of the output register through the multiplexer onto the bus.

All three select lines generate an I BUS ENABLE RT signal when the register is addressed which is used by the bus control to permit a proper master/slave relationship (Figure 3-63). If the LPSDR-A is not installed, the slave signal is inhibited when these registers are addressed and the computer traps.

3.5.3 Input Register Write

The user cannot write ones into the input register but can write zeroes. A zero is written into the input register by writing a 1 into a bit that clears the bit. Signals LD IN HIGH and LD IN LOW are ANDed with each individual bit via a multiplexer to clear the bit in the input register (Figure 3-65).

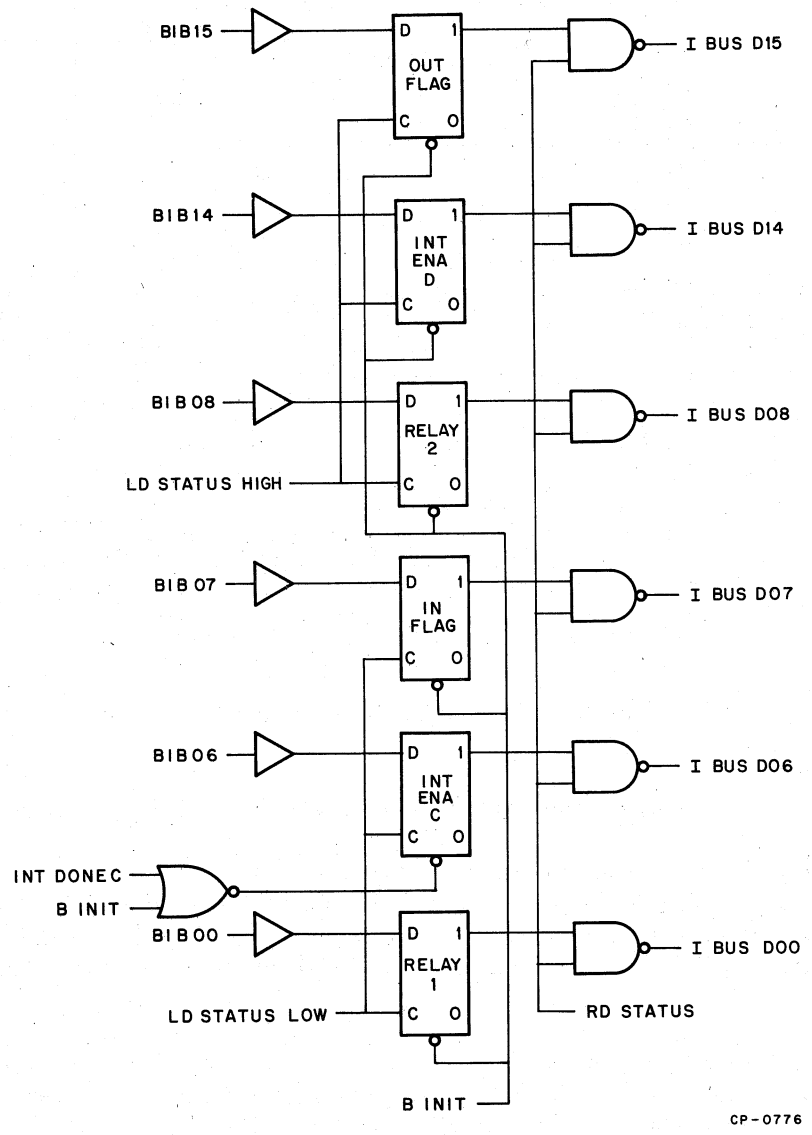

Figure 3-63 LPSDR-A Status Register

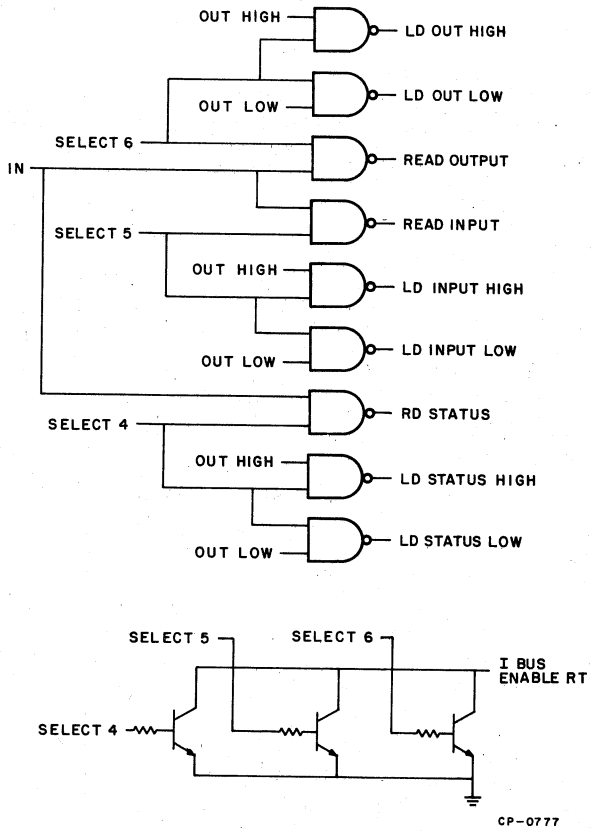

Figure 3-64 Address Control Signal Gating

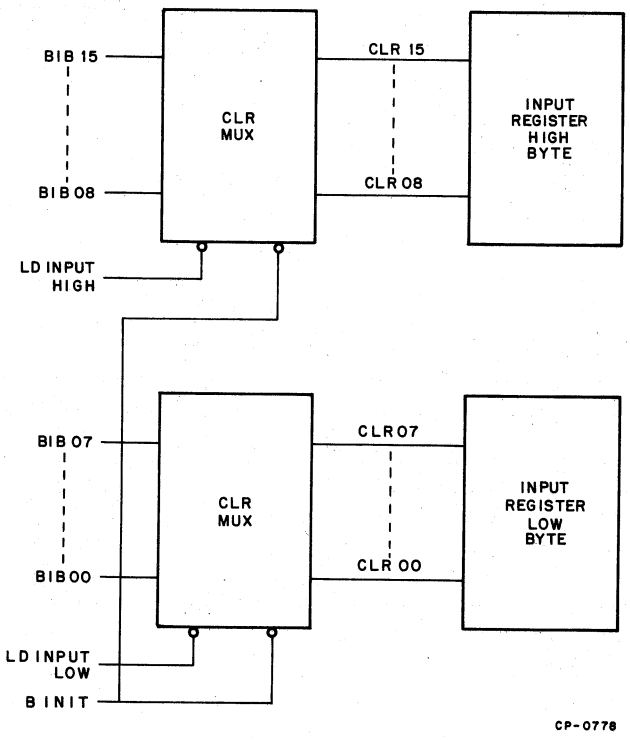

Figure 3-65 Clear Multiplexers

3.5.4 Input Register Data

When external data is applied to the LPSDR-A option, the normally negative going data bit pulse clocks the input register bit on the falling edge and sets the bit. (Figure 3-66). Bits 15 and 14 (Figure 3-66) accept either polarity, depending on the configuration of jumpers W16, W16A, W17 and W17A. Table 3-20 lists bit polarity versus jumper configuration.

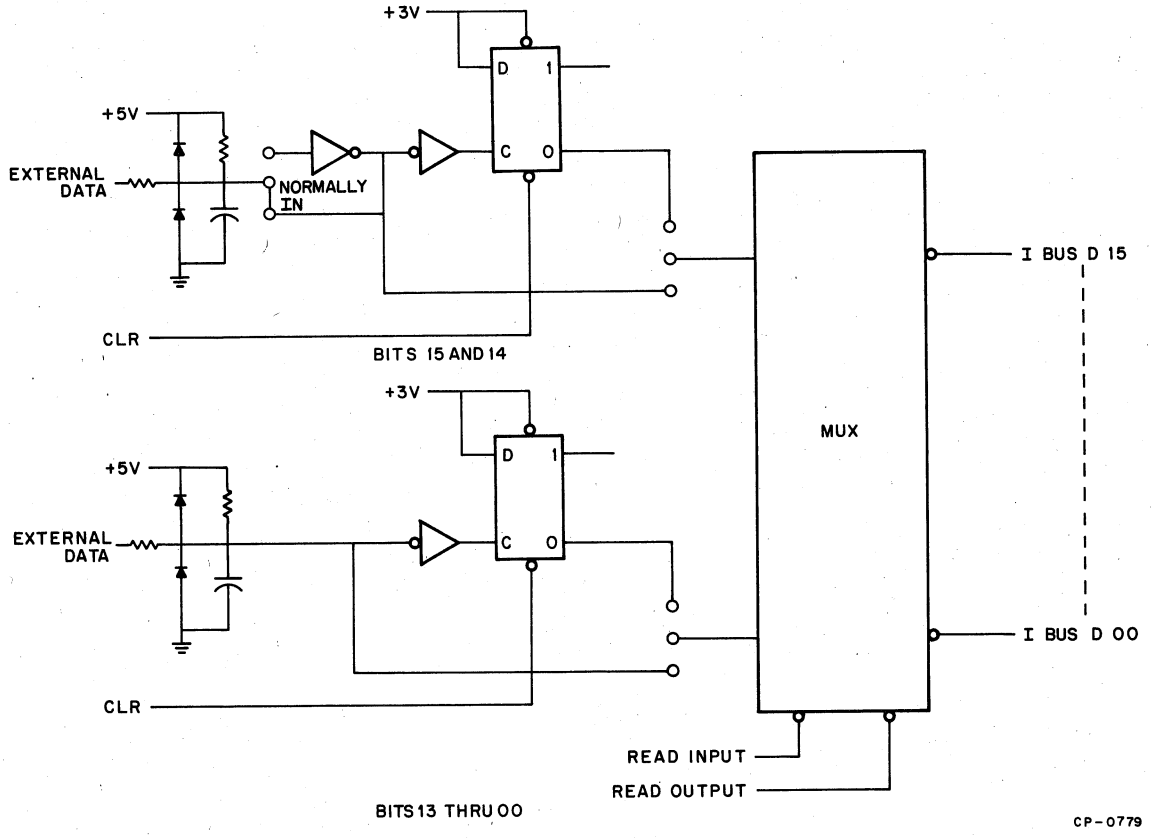

Figure 3-66 Input Register

Table 3-20
Bit 14 and 15 Jumpers

Bit	Jumper		Signal Polarity (True)
	Installed	Removed	
15	W16A	W16	+3 V (1)
15	W16	W16A	GND (2)
14	W17A	W17	+3 V (1)
14	W17	W17A	GND (2)

(1) +5 V max
(2) +0.4 V max

Once data has clocked the flip-flop, one of three modes may be selected via jumpers W00–W15, W00A–W15A, and switches SW15 through SW00 (Figure 3-67). Selecting jumpers W15 through W00 and placing switches SW15 through SW00 in the on position places the LPSDR-A in the Stimulus mode. In this mode any bits (falling edge) entering from an external device are latched and can cause an interrupt.

Word Transfer mode occurs only when jumpers W00A through W15A are installed, W15 through W00 are removed, and SW15 through SW00 are in the off position. In this mode the latches are ignored and input interrupts may only occur because of the signal EXT NEW DATA READY.

Mix mode is a combination of the Stimulus and Word Transfer modes, where the user application defines the jumpers and switches used (Table 3-21).

Both input and output registers are multiplexed onto the I BUS by READ INPUT or READ OUTPUT signals respectively.

Table 3-21
Mode Selection Jumpers

Input Bit	Installed Jumper	Removed Jumper	Stimulus	Mode Word Transfer	Mix
15	W15	W15A	X		Either
	W15A	W15		X	
14	W14	W14A	X		
	W14A	W14		X	
13	W13	W13A	X		
	W13A	W13		X	
12	W12	W12A	X		
	W12A	W12		X	
11	W11	W11A	X		
	W11A	W11		X	
10	W10	W10A	X		
	W10A	W10		X	
09	W09	W09A	X		
	W09A	W09		X	
08	W08	W08A	X		
	W08A	W08		X	
07	W07	W07A	X		
	W07A	W07		X	
06	W06	W06A	X		
	W06A	W06		X	
05	W05	W05A	X		
	W05A	W05		X	
04	W04	W04A	X		
	W04A	W04		X	
03	W03	W03A	X		
	W03A	W03		X	
02	W02	W02A	X		
	W02A	W02		X	
01	W01	W01A	X		
	W01A	W01		X	
00	W00	W00A	X		
	W00A	W00		X	Either

(**NOTE**: Jumpers W15 and W15A through W00 and W00A must never be simultaneously installed.)

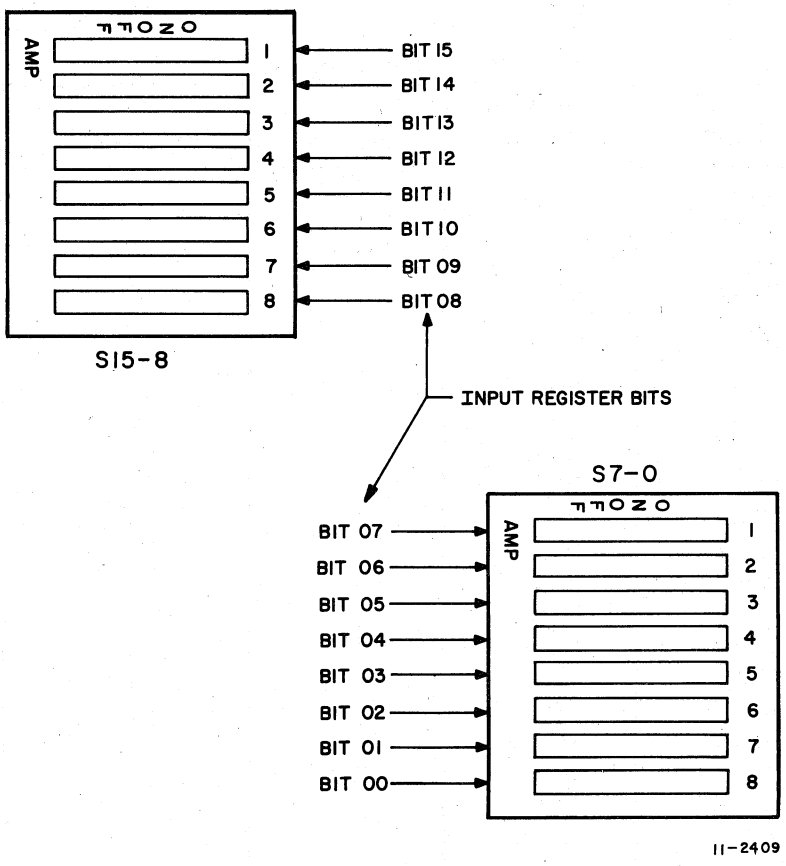

Figure 3-67 Input Register Interrupt Switches

3.5.5 Output Register Write

To send data to an external device, LD OUT LOW and LD OUT HIGH signals are generated, which load the low, high, or both bytes from the bus (Figure 3-68). Each output is protected against harmful voltages (±20 V) by 47 ohm fusable resistors.

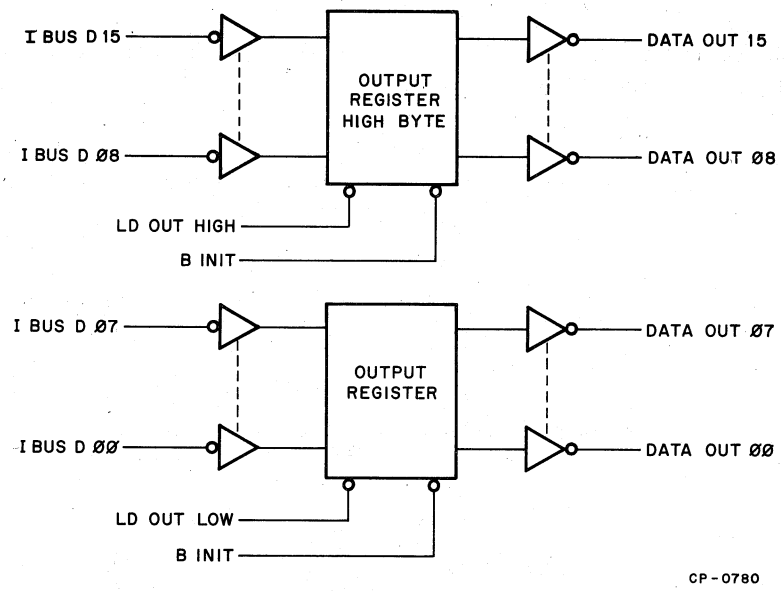

Figure 3-68 Output Register

3.5.6 Input Control and Interrupt

When data becomes available, the external device sends a pulse, EXT NEW DATA READY, which tells the LPSDR-A that data is being transmitted. This signal (EXT NEW DATA READY) should only be used in Word Transfer and Mix modes. EXT NEW DATA READY direct sets the IN FLAG and if INT ENA C is set, the INT C flag sets telling the bus control that data has been sent to the LPSDR-A. When the bus control acknowledges the interrupt, an input INT DONE C is sent which clears the input INT ENA C flip-flop and the INT C flip-flop (Figure 3-69).

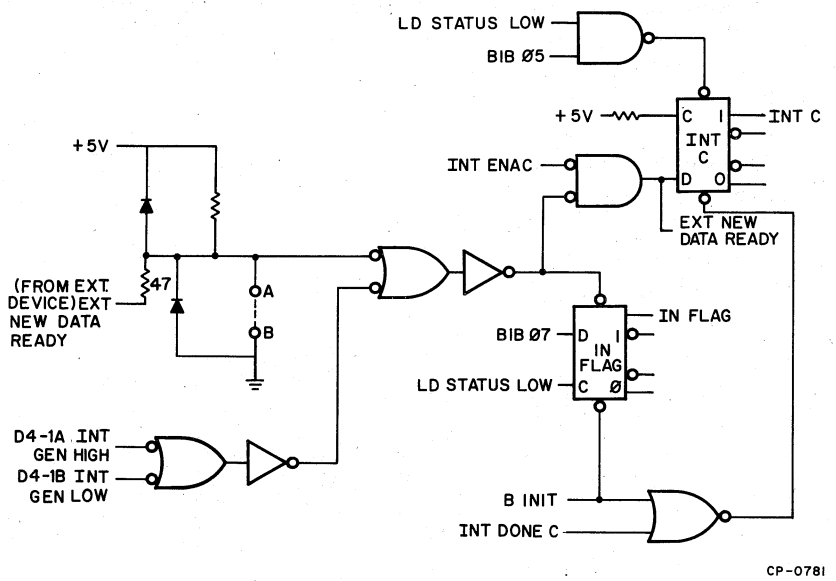

Figure 3-69 Interrupt Circuit

When in the Stimulus mode the signal EXT NEW DATA READY should not be used. When data becomes available from the external device those switches that are in the on position may cause an interrupt by either the INT GEN HIGH or INT GEN LOW signal. At least one switch must be on for an interrupt to occur. Once either INT GEN HIGH or INT GEN LOW has been generated, the process is the same as for the signal EXT NEW DATA READY (Figures 3-69 and 70).

Split lugs A, B, C, and D provide the user with the option of adding capacitance for noisy signals. Maintenance mode bits 05 and 13 provide the user with testing methods.

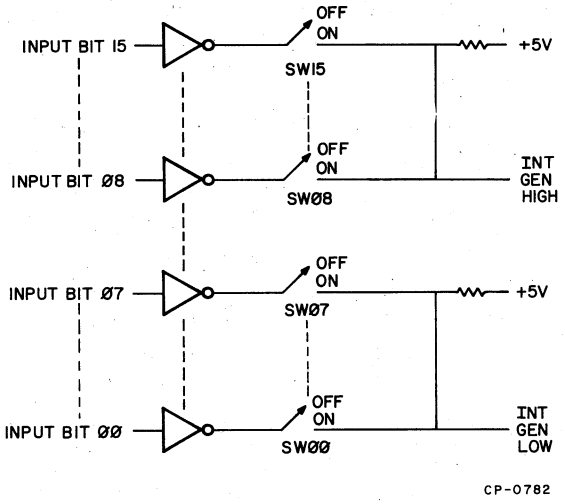

Figure 3-70 LPSDR-A Interrupt Structure for Input Register

Once the input has been sensed and a flag or interrupt has occurred, the user may read the input lines. A READ INPUT signal causes a 1 μs pulse to be sent to the external device to tell it that data has been read and new data may now be sent. The pulse (INTL DATA ACCEPT) may be of either polarity as defined by jumper W19 or W19A (factory set with W19) (Figure 3-71). Pulse width is defined by the factory-installed resistors and may be changed by removing the 10K resistor and installing an alternate resistor across split lugs E and F. Table 3-22 lists pulse widths available with various resistances. A formula which may be used to determine other pulse widths is provided below.

$$92.4R_t + 6.6 = T_w$$

where: T_w = Pulse width in nanoseconds (ns)
R_t = Resistance in kilohms (10^3)

and R_t range = 1.1k min.
= 108k max.

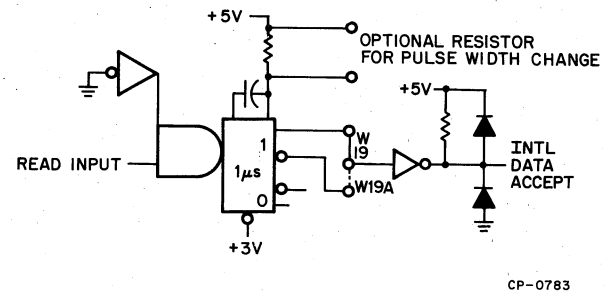

Figure 3-71 INTL DATA ACCEPT Circuit

Table 3-22
Pulse Width Resistors for INTL DATA ACCEPT

Resistance (k)	Pulse Width (ns)
5	500
10	1000
20	1900
50	4700

NOTE:
Capacitor must remain 330 pF for table or formula to apply.

3.5.7 Output Control and Interrupt

Loading the output register causes either an LD OUT HIGH and/or LD OUT LOW to generate a 1 μs pulse called INTL NEW DATA READY (Figure 3-72) which can be used to load the external devices input register with the data contained in the output register. Pulse polarity may be changed with jumpers W18 and W18A.

Pulse polarity is factory wired for a negative (GND) pulse. Pulse width is defined by the 10K resistor and may be changed by removing the 10K resistor and installing another resistor (Table 3-22) across split lugs H and J.

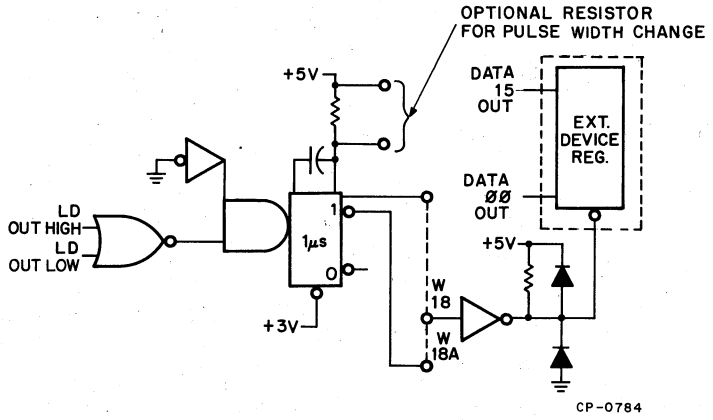

Figure 3-72 INTL NEW DATA READY Circuit

Data output from an external device is acknowledged by an EXT DATA ACCEPT pulse, which directly sets the OUT FLAG (status register bit 15) as shown in Figure 3-73. If the output interrupt is enabled, the INT D flip-flop will be qualified. The flip-flop output is then sent to the bus control, which processes the interrupt. Upon completion, a done signal (INT DONE D) is returned to the digital I/O to clear the interrupt flip-flop and enable the processor to load new data into the output register.

3.5.8 Relays

The two relays associated with the LPSDR-A digital I/O are located on the front panel of the LPS11-S and are controlled by status register bits 00 and 08 (Figure 3-74). The relay outputs are applied to a switching transistor which provides isolation between the relays and the external device. When the transistor is biased off, the relay is open; when the transistor is turned on, the relay is closed. The diode prevents a positive voltage spike from damaging the transistor on turn-off.

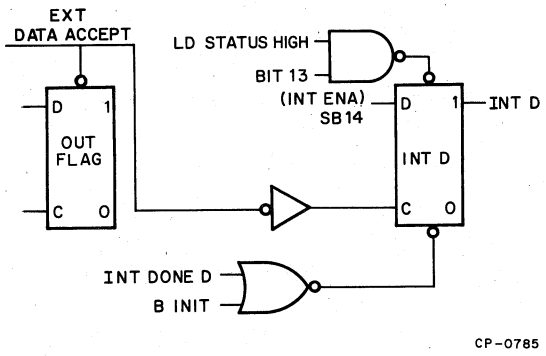

Figure 3-73 Output Register Data Accept

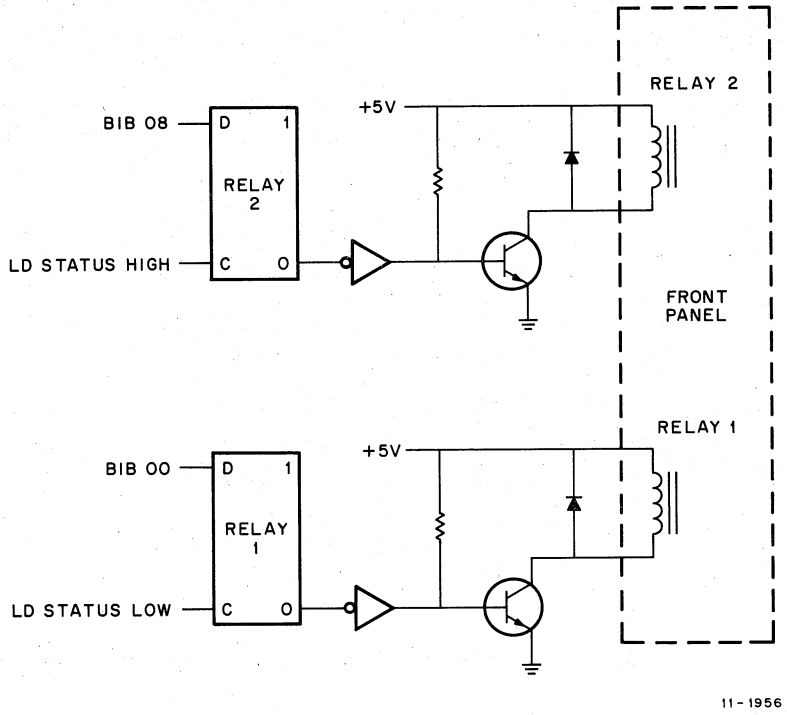

Figure 3-74 Relays

3.5.9 Programming

The LPSDR-A digital I/O option consists of three device registers. These registers and their bit assignments are illustrated in Figures 3-75 and 3-76. Descriptions of the bit functions appear in Tables 3-23, 3-24, and 3-25.

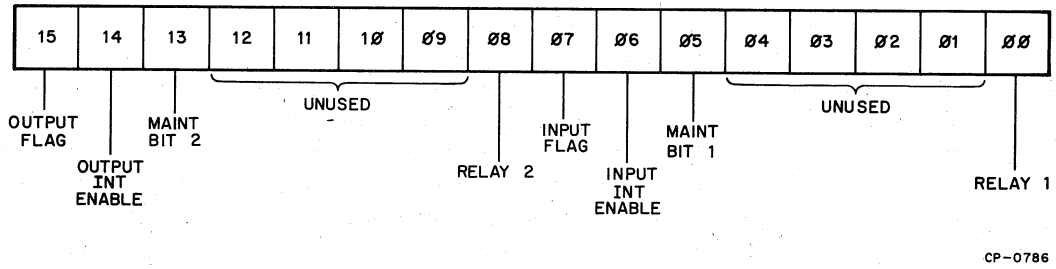

Figure 3-75 LPSDR-A Status Register Bit Assignments

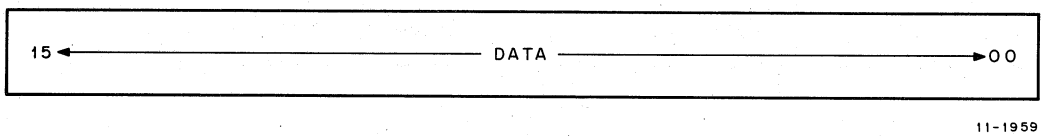

Figure 3-76 Output or Input Register Bit Assignments

Table 3-23
Output Register Bit Functions

Bit	Name	Meaning and Operation
15	Output Flag	Sets when device sends EXTERNAL DATA ACCEPT pulse signifying that data is taken from Output register.
14	Output Interrupt Enable	Permits setting of Output flag to cause interrupt.
13	Maintenance Bit 2	Sets Output interrupt for maintenance purposes.
12–9	Unused	
8	Relay 2	Setting or clearing causes relay 2 to close or open, respectively.
7	Input Flag	Sets when device sends EXTERNAL NEW DATA READY signal signifying that data has been placed in Input register.
6	Input Interrupt Enable	Permits setting of Input to cause interrupt.
5	Maintenance Bit 1	Sets Input interrupt for maintenance purposes.
4–1	Unused	
0	Relay 1	Setting or clearing causes relay 1 to close or open, respectively.

Table 3-24
Output Register Bit Functions

Bit	Name	Meaning and Operation
15–00	Data	These bit positions contain information loaded from the Unibus for transfer to the external device. When set, a bit represents a logical 1 (0 V); when cleared, a logical 0 (+3 V). When this buffer is loaded by the processor, a signal is generated simultaneously and applied to the external device to inform it that data is ready for transfer. This register can be loaded or read by the central processor.

Table 3-25
Input Register Bit Functions

Bit	Name	Meaning and Operation
15–00	Data	These bit positions receive information from the external device.
15, 14	Data	These bits may accept a ZERO or a ONE as a logical 1 (depending on installation of jumpers W16, W16A, W17, and W17A). This is a read only register. Bits may be masked or cleared by setting the appropriate bit and loading the input register (bit set causes bit to clear).

3.6 POWER SUPPLY

3.6.1 Block Diagram Discussion

The power supply (Figure 3-77) can be operated from a source of 115 or 230 Vac, single-phase, 60 or 50 Hz, depending upon the configuration of the power control unit, which contains patch jumpers for the fan and power transformer primary, a circuit breaker, and RFI capacitors.

The patch jumpers make it possible to connect the primary windings of the transformer in parallel to permit operation of the supply from a 115 Vac source, or to connect the windings in series to enable operation of the supply from a 230 Vac source. The circuit breaker provides current overload protection. The RFI capacitors reduce radio frequency interference in the ac line input.

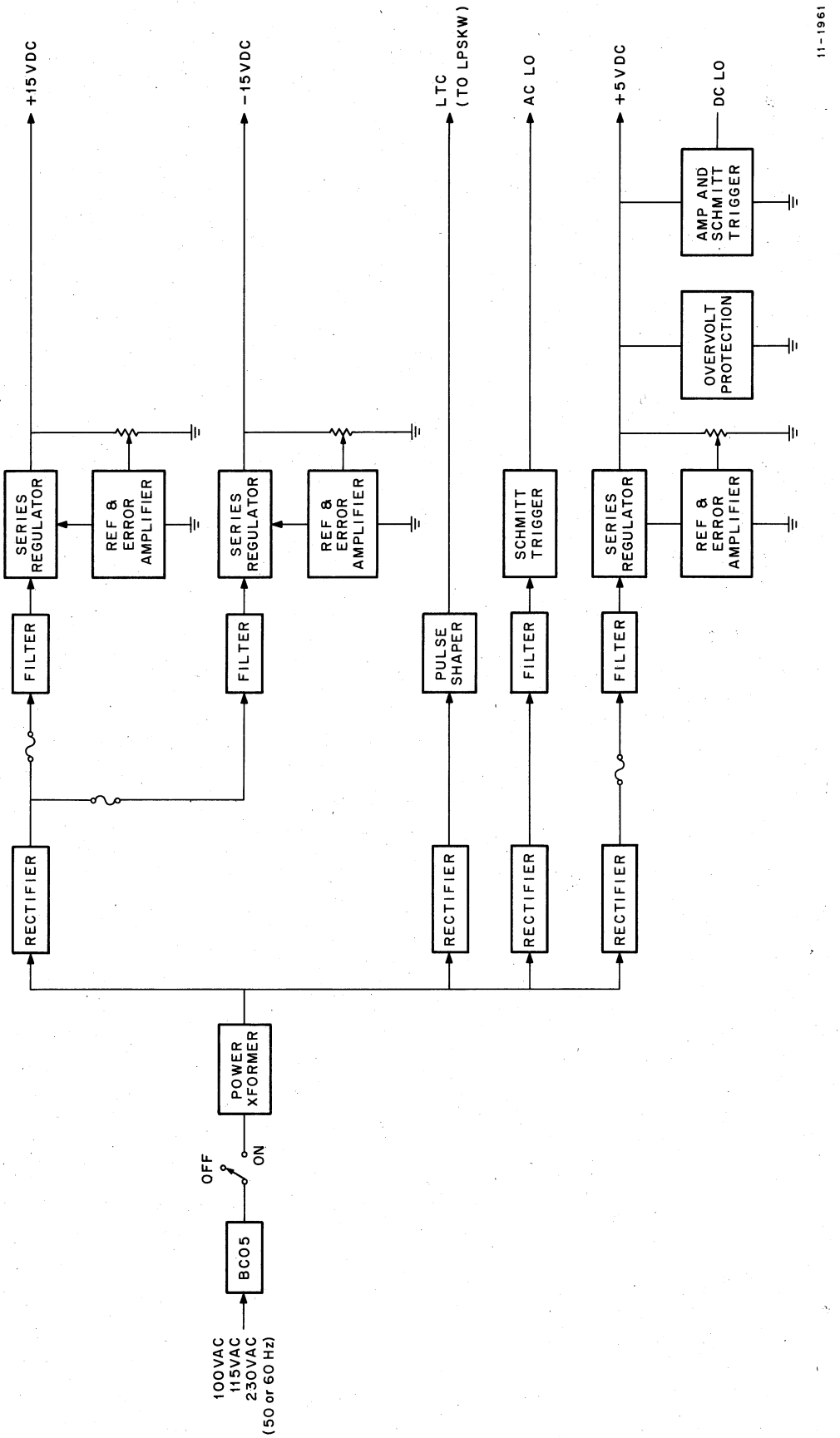

Figure 3-77 Power Supply Block Diagram

CHAPTER 4
ADJUSTMENT AND CALIBRATION

4.1 LPSVC DISPLAY CONTROL

The LPSVC display control option consists of two modules: the M7019 Scope Control module and the A625 Dual Digital-to-Analog Converter (DAC) module. The M7019 Scope Control module makes it possible to jumper-select various displays as shown in Note 2 of drawing D-CS-M7019-0-1, sheet 3. The A625 DAC module provides jumper selection of the various gains and offsets, and also provides an offset and gain adjustment for each DAC.

Table 4-1 lists the jumper configurations required for each of the various CRT display scopes that can be controlled by the LPSVC option. All jumpers are designated on the modules. Both modules are jumpered at the factory for the standard VR14 and VR20 configurations listed in Table 4-1.

NOTE

In Table 4-1, the presence of an "X" indicates a jumper in place on the M7019 or A625 modules.

Tektronix scopes have provisions for variable attenuation. To obtain a better signal-to-noise ratio, an attenuation factor is recommended for each Tektronix scope. If an attenuation change becomes necessary, refer to the appropriate Tektronix instruction manual for the particular display being controlled.

4.1.1 M7019 Scope Control Jumper Data

Table 4-2 indicates how jumpers A, B, C, and D are used to vary the gain and offset of the intensify signal.

The voltages listed in Table 4-2 are the approximate voltages for the various intensify pulse output capabilities of the M7019 module. Z output voltages are peak-to-peak voltages.

- For a negative intensify signal output, connect jumper E.
- For a positive intensify signal output, connect jumper F.

When using the two-color VR20 display, the delay after a load for red varies from the delay after a load for green. Table 4-3 shows delay time variations for the intensify pulse after a load has been issued.

Table 4-1
LPSVC Display Control Jumper Connection Data

		Standard Module	Digital		Tektronix						
			VR14	VR20	601	602	603	604	611	613	503
Recommended Attenuation Factor*		NA	NA	NA	5	5	5	5	5	5	
M7019 Jumper Arrangement	D-W1	X	X	X							X
	W2				X		X		X	X	
	A-W3	X	X	X							
	B				X	X	X	X	X	X	
	C										X
	E				X	X	X	X	X	X	X
	F-W4	X	X	X							
	G-W5	X	X	X		X		X			
	H				X		X		X	X	X
A625 Jumper Arrangement	W1										
	W2	X	X	X	X	X	X	X	X	X	X
	W3	X	X	X	X	X	X	X	X	X	X
	W4	X	X	X					X	X	X
	W5				X	X	X	X			
	W6	X	X	X					X	X	X
	W7										
	W8	X	X	X	X	X	X	X	X	X	X
	W9	X	X	X	X	X	X	X	X	X	X
	W10	X	X	X					X	X	X
	W11				X	X	X	X			
	W12	X	X	X					X	X	X

*Refer to the associated Tektronix manual for appropriate attenuation factors.

Table 4-2
M7019 Gain and Offset

Jumper Placement	Z Output With Jumper D-W1	Z Output Without Jumper D-W1	Displays
A	-1.25 to +4.5V	NA	VR14, VR20
B	NA	-0.5 to +1.25V	Tektronix 601, 602, 603, 604, 611, and 613
C	-1 to +4V	NA	Tektronix RM503

Table 4-3
VR20 Delay Time Variations

Jumper Placement		GREEN L	GREEN H
In	Out		
G-W5*	H	20 μs	11 μs
H**	G-W5	22 μs	NA***

*The G jumper enables the variation in delay to occur.
**The H jumper fixes the delay.
***The signal GREEN H has no effect if jumper H is in place.

4.1.2 A625 DAC Jumper Data

Table 4-4 shows the jumper configuration required to select the various output voltage ranges provided by the A625 module.

Table 4-4
A625 Voltage Gain Selection

Jumper Placement		Gain	Output Voltage	
X Output	Y Output		Bipolar	Unipolar
W8	W2	20	±10V	NA
W8 and W9	W2 and W3	10	±5V	0 to -10V
W7	W1	1	±0.5V	0 to -1V

Table 4-5 shows the jumper configurations that select whether operation is to be unipolar or bipolar in conjunction with the gain selection jumper configurations shown in Table 4-4.

Table 4-5
A625 Bipolar/Unipolar Selection

Output Polarity	Jumper Placement	
	X Output	Y Output
Unipolar	W11	W5
Bipolar	W10	W4

Table 4-6 defines the various jumper functions.

Table 4-6
A625 Jumper Functions

Jumper	Function	Reference
W1 or W7	Varies DAC gain	Table 4-4
W2 or W8	Varies DAC gain	Table 4-4
W3 or W9	Varies DAC gain	Table 4-4
W4 or W10	Selects bipolar output	Table 4-5
W5 or W11	Selects unipolar output	Table 4-5
W6 or W12	Prevents VR14 or VR20 from being overdriven. Clamps DAC output to +6.2V	Table 4-5

4.1.3 A625 Offset and Gain Adjustments

The A625 is a dual-channel digital-to-analog converter. In the LPSVC option, it is used to drive the X and Y axes of a point plot display. When either its X or Y holding register is loaded with a 12-bit binary number, it is immediately converted to an analog level, which is driven to the deflection amplifier in the display.

When the module is shipped from the factory, it is jumpered and calibrated for use with the VR14 and VR20 displays, with a bipolar gain of 10 and an output range of from -5V to +5V. Each bit of the 12-bit register represents 2.5 mV of analog output.

It is possible to recalibrate the A625, if necessary. A DVM with an accuracy of 1 mV or better is needed, using the following procedure:

a. Offset Adjustments – Load binary 4000 into the calibration axis. This can be done by depositing it into address 770420 for X or 770422 for Y. The output should measure 0V. If it does not, adjust the offset potentiometer of the axis being calibrated (Figure 4-1).

b. Gain Adjustment – Deposit binary 0000 into the calibrating axis. The output should be -5V ± 1 mV. If it is not, adjust the gain potentiometer of the axis being calibrated. Repeat the offset adjustment described in a., above, and, if necessary, the gain adjustment.

   Check the upper end. Deposit binary 7777 into the calibrating axis. The output should be 4.997V ± 2.5 mV. Check output symmetry vs binary input according to Table 4-7.

4.2 LPS11-S ANALOG SYSTEM

4.2.1 Initial Conditions

The LPS11-S analog system calibration procedure depends upon each module in the system having been previously adjusted according to Table 4-8.

The modules are individually calibrated at the factory to the conditions specified in Table 4-8, using in-house module testers or, if the testers are not available, by performing either of the LPS11-S Analog Board Calibration Procedures.

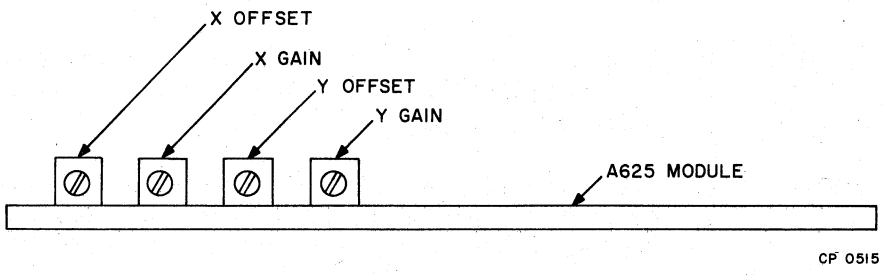

Figure 4-1 Location of A625 Offset and Gain Adjustments

Table 4-7
Output Symmetry vs Binary Input

Binary Input	Analog Output (±2.5 mV)
0000	-5.0V
1777	-2.5V
0000	0.0V
3000	+2.5V
7777	+4.997V

Table 4-8
Initial Calibration Specifications
for LPS11-S Analog System Modules

Module	Initial Adjustment Specification
A242 Preamplifiers	All four channels on each module are initially adjusted so that an exact ±1V input provides an exact ±5V output, and an optimum common mode rejection ratio (CMRR) has been obtained.
A407 Multiplexer	The 310 amplifier balance potentiometer has been adjusted for zero offset.
A406 Sample-and-Hold	Offset potentiometer R28 has been adjusted for zero offset. This is performed with 0V input on both the signal input (pin A1) and the system offset input (pin J1).
A804 A/D Converter	The word length switch is set for 12-bit conversion. The clock time is set for 19 μs conversion. The gain and offset potentiometers are set for the 0000-to-0001 transition at V_{in} = -1.25 mV and the 7776-to-7777 transition at V_{in} = -9.99625V.

4.2.2 Test Equipment and Diagnostic Programs

The following test equipment and diagnostic programs are required to calibrate the LPS11-S analog system:

a. LPS11-S with LPSAD-12 option installed

b. PDP-11 system with at least 4K of memory

c. LPS diagnostic MAINDEC-11-DZLPC-A

d. Electronic Development Corporation dc Voltage Source (EDC) VS-11N, or equivalent.

In some cases, the EDC may tend to provide a noisy output when used with positive voltage ("-,0,+" output switch in the "+" position). If this occurs, use the EDC with the output switch in the "-" position with the LPS11-S input leads reversed to provide a positive LPS input voltage.

NOTE
Always leave the EDC power line floating; connect the EDC chassis ground directly to the LPS11-S chassis ground, using a 3-wire input cable, as shown in Figure 4-2.

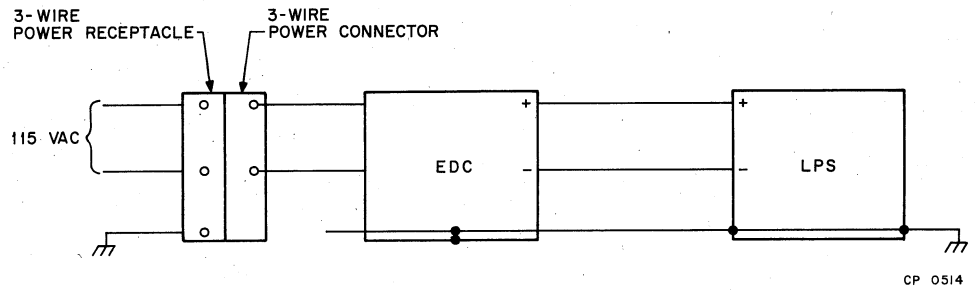

Figure 4-2 EDC Voltage Source, Showing Floating Power Lines

4.2.3 Single Sample-and-Hold System Calibration

The calibration procedure for single sample-and-hold systems is as follows:

1. Connect EDC output to channel 0 input.

2. Load system diagnostic and select calibration test (C). Select channel 0 by leaving Switch register at 000000_8.

3. With EDC voltage set per line A of Table 4-9, adjust A406 Sample-and-Hold module potentiometer R27 (right-hand side) to obtain, as nearly as possible, the 0000-to-0001 transition as viewed on the LED display.

4. Adjust A804 A/D Converter module potentiometer R16 (right-hand side) for the exact point of 0000-to-0001 transition (50-50 duty cycle).

NOTE

It is important to get as close as possible to the 0000-to-0001 transition point with the A407 potentiometer (R27) before trimming up with the A804 potentiometer (R16) to minimize subsequent temperature drift. In no instance should it be necessary to take out more than one or two counts using A804 potentiometer R16.

5. Set the EDC voltage as indicated on line B of Table 4-9, and adjust A804 potentiometer R15 (left-hand side) for the exact point of the 7776-to-7777 transition (50-50 duty cycle). Recheck the adjustments of steps 3 through 5, if necessary.

Table 4-9
Sample-and-Hold System Calibration Data

Test	Input Voltage		Adjustment Potentiometers	Transition Point Viewed on LED Display
	With LPSAG Preamps	Without LPSAG Preamps		
A	-0.99975V	-4.99875V	A406: R27 A804: R16	0000/0001
B	+0.99925V	+4.99625V	A804: R15	7776/7777

4.2.4 Dual Sample-and-Hold System Calibration

The LPSSH option provides a dual sample-and-hold capability for the LPS11-S analog system. The system calibration procedure is the same as that described for a single sample-and-hold system, with the following exceptions:

1. When adjusting for the 0000-to-0001 transition as described in Paragraph 4.2.3, use A406 potentiometer R27 for the coarse adjustment as before; however, use A406 potentiometer R28, rather than R16, for the fine adjustment.

2. With the EDC connected to channel 0, perform the 0000-to-0001 transition adjustments on A406 Sample-and-Hold module number 1, and the 7776-to-7777 transition adjustments on the A804 as described in step 5 of Paragraph 4.2.3.

3. With the EDC connected to channel 10_8 and the Switch register set to 000010_8, perform the 0000-to-0001 transition adjustments described in step 1 of Paragraph 4.2.3.

4. With the EDC connected to channel 10_8 and the EDC output voltage set at +0.75V for a system with preamplifiers, or set at +3.75V for a system without preamplifiers, the LED display should read 7000, with a ±2 tolerance. If this is not the case, perform the procedures described in steps 5 and 6, below.

5. Set the EDC voltage for +0.99625V for a system with preamplifiers or for +4.98125V for a system without preamplifiers.

6. Adjust A804 potentiometer R15 for both channel 0 and channel 10_8 as close as possible to the 7770-to-7771 transition.

Because of slight differences in gain between multiplexer/sample-and-hold number 1 and multiplexer/ sample-and-hold number 2, it may be necessary to adjust for one channel high and the opposite channel low. For example, channel 0 may be at the 7767-to-7770 transition and channel 10_8 may be at the 7771-to-7772 transition. Optimum adjustment of A804 potentiometer R15 will result in channels 0 and 10_8 bracketing the 7770-to-7771 transition with equal and opposite errors.

4.2.5 Switch Gain Multiplexer Calibration

The A408 module contains three zero adjustments: RTO coarse, RTO fine, and RTI. The RTO (referred-to-output) pots should only be adjusted at a gain of 1 (channels 0–17), where amplifier output effects predominate. The RTI (referred-to-input) pot should only be adjusted at a gain of 64 (channels 60–77), where amplifier input effects predominate.

It is always preferable to perform the A408 adjustments on the A408T Tester. An A408 module which has been properly adjusted on the A408T Tester needs no further adjustment in a properly-adjusted LPS11. Adjustment of an A408 module in the LPS should only be done if an A408T Tester is not available. Adjustment of an A408 in an LPS should be done without pre-amps. If the LPS contains pre-amps, they should be temporarily replaced by jumper cards and reinstalled after A408 adjustments are completed. If calibration of the LPSAD-12 is in doubt, it should be checked before replacing the A407 multiplexer with the A408. In order to minimize the effects of noise, the RTI (G=64) adjustment should be done using the *LPS Diagnostic Repeatability Test,* with CPU front console switch 13 in the up position, so that the LPS LED's display the average value of each burst of 512 conversions. The RTO (G=1) adjustment may obtain its LED display using either the Repeatability Test with switch 13 up or the Calibration Test.

4.2.5.1 EDC Voltage Source Available

1. Connect EDC to channel 0 input for a 0–7 A408 or channel 10 input for a 10–17 A408 (10–17 A408 need not be adjusted except for a dual sample-and-hold configuration – LPSSH installed).

2. Set EDC voltage at +1.25 mV. Use the diagnostic to monitor channel 0 or 10 (G=1).

3. Set fine RTO pot (R24) near its center point.

4. Adjust coarse RTO pot (R25) for display as close as possible to the 4000/4001 (50-50) transition.

5. Adjust fine RTO pot (R24) for exact 4000/4001 (50-50) transition.

6. Disconnect EDC and use a shorting plug to force a zero input on channel 0 or 10.

7. Use the diagnostic to monitor channel 60 or 70 (G=64).

8. Set RTI pot (R22) for display of 4000.

9. Recheck channel 0 or 10 (G=1) and repeat if necessary.

4.2.5.2 EDC Not Available – If an EDC is not available, the channel 0 or 10 (G=1) adjustments should be performed using a shorting plug to force a zero input. In this case, the RTO pots should be adjusted for the middle of the 4000 output code instead of the 4000/4001 transition.

4.2.5.3 Pre-amp Adjustments with SG – The offset of the LPSAG and LPSAG-VG pre-amps is adjusted on the pre-amp module tester to a tolerance commensurate for use with the A407 Fixed Gain Multiplexer module (operating at a gain of 1). This can cause significant offsets on those channels for which pre-amps are installed, when the A408 multiplexer is operated at higher gains. For example, a 500 μV offset at the output of a pre-amp, while only 0.2 LSB at G=1, equals approximately $13_{10}=15_8$ LSB at G=64.

This offset should be adjusted out for each pre-amp channel, using the pre-amp balance adjust pot, while operating in the LPS. The channel input should be set to zero with a shorting plug. The LPS Diagnostic Repeatability Test should be run at G=64, with CPU front console switch 13 in the up position, so that the LPS LED's display the average value of each burst of 512_{10} conversions. The balance adjust pot should be set for a display of 4000.

CHAPTER 5
SYSTEM TROUBLESHOOTING

This chapter provides troubleshooting data that will aid in locating the cause of an LPS option problem. The data is based on the use of two diagnostic programs:

MAINDEC-11-DZLPD-A
MAINDEC-11-DZLPC-A

Table 5-1 lists the parts of these diagnostic programs that are used to troubleshoot specific LPS options.

Table 5-1
Diagnostic Programs for LPS Options

LPS Option	Diagnostic MAINDEC-11-	Part
LPSKW Real-Time Clock	-DZLPD-A	A
LPSDR Digital I/O	-DZLPD-A	B
LPSVC Display Control	-DZLPD-A	C
LPSAD-12 A/D Converter	-DZLPC-A	A
LPSAD-NP DMA Option	-DZLPC-A	B

The troubleshooting data is presented in a series of five tables (Tables 5-2 through 5-6), one for each of the options listed in Table 5-1. Each table lists the subtests for that option. Listed below each option subtest heading are the signals that could possibly cause failure during that subtest. The lists include the logic schematic that shows where the signal is developed, the signal mnemonic, the grid location where the logic is shown on the schematic, and the IC pin assignment.

NOTE
To use this troubleshooting data effectively, it is necessary to be thoroughly familiar with the LPS11-S theory of operation (Chapter 3) and the use of the diagnostic programs (Chapter 2), and to understand the logic schematics well enough to trace a signal back to the source of trouble.

Table 5-2
LPSKW Data: DZLPD, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
KWT0–KWT4				
	PRESET BUFFER REGISTER	D3-2	BCD-2	
	LOAD BUF H	D3-1	C-1	E34-13
	PLD BUF H	D3-3	A-6	E37-4
	STALL H	D3-3	B-6	E38-10
	BUFFERS MUX	D3-2	ABCD-4	
	CKBF BF (1) L (no signal)	D3-1	D-3	E28-6
	DATA BUS MUX OUT	D3-2	ABCD-6	
	RD BUF L	D3-3	A-6	E27-11
KWT5				
	ENA CT (1) H	D3-3	B-1	
	LD STATUS LB H	D3-3	A-7	E32-11
	DATA BUS MUX OUT	D3-2	B-6	
	RD STATUS L	D3-3	A-7	E27-8
KWT6–KWT10				
	LOW STATUS REGISTER	D3-3	C-2	
	LD STATUS LB H	D3-3	A-7	E32-11
	DATA BUS MUX OUT	D3-2	AB-6	
	RD STATUS L	D3-3	A-7	E27-8
KWT11–KWT15				
	HIGH STATUS REGISTER	D3-3	D-2	
	LD STATUS HB	D3-3	A-7	E32-8
	DATA BUS MUX OUT	D3-2	CD-6	
	RD STATUS L	D3-3	A-7	E27-8
KWT16				
	FLAG 1 (0) H	D3-3	A-4	E21-8
	LD STATUS LB H	D3-3	A-7	E32-11
	DATA BUS MUX OUT	D3-2	B-6	
	RD STATUS L	D3-3	A-7	E27-8
KWT17				
	FLAG 2 (1) H	D3-3	A-5	E21-5
	LD STATUS HB H	D3-3	A-7	E32-8
	DATA MUX OUT	D3-2	D-6	
	RD STATUS L	D3-3	A-7	E27-8
KWT18				
	FLAG 2 (1) H (never set)	D3-3	A-5	E21-5
	ST PULSE (1) L (no signal)	D3-1	C-4	E41-6
	ST1 L (no signal)	D3-3	B-4	E46-4

Table 5-2 (Cont)
LPSKW Data: DZLPD, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
KWT19				
	FLAG 2 (1) H	D3-3	A-5	E21-5
	ST PULSE (1) L	D3-1	C-4	E41-6
	LD STATUS HB H	D3-3	A-7	E32-8
KWT20				
	ENA CT (1) H	D3-3	B-2	E26-9
	ST PULSE (1) H	D3-1	C-4	E41-5
	LD STATUS HB H	D3-3	A-7	E32-8
	ST ENA (1) H	D3-3	D-2	E5-7
KWT21				
KWT22				
	FLAG 1 (1) H	D3-3	B-4	E21-9
	CKBF BF (1) H	D3-1	C-3	E28-5
	LD STATUS HB H	D3-3	A-7	E32-8
KWT23–KWT25				
	COUNTER REGISTER	D3-2	BCD-8	
	LD CT L	D3-1	A-3	E40-8
	P LD BUF H	D3-3	A-7	E37-4
	CKBF BF (1) L	D3-1	C-3	E28-6
	LOAD BUF H	D3-1	C-2	E34-13
	BUFFER MUX	D3-2	ABCD-4	
KWT26				
	LOAD BUF H	D3-1	C-1	E34-13
	CKBF BF (1) L	D3-1	C-3	E28-6
	COUNT L	D3-1	C-1	E43-5
	1 MHZ L (maintenance)	D3-1	B-4	E40-6
	COUNTER REGISTER	D3-2	BCD-8	
	RD STATUS L	D3-3	A-7	E27-8
	OUTPUT MUX	D3-2	ABCD-6	
	RATE 0 (1) H	D3-3	C-1	E10-14
KWT27				
	COUNTER REGISTER	D3-2	BCD-8	
	A OV L	D3-2	D-8	E6-12
	COUNT L	D3-1	C1	E43-5
	FLAG 1 (1) H	D3-3	A4	E21-9
KWT30				
	LOAD BUF H	D3-1	C-1	E34-13
	COUNT L	D3-1	C-1	E43-5
	100KHZ L	D3-1	B-4	E25-13
	RATE 1 (1) H	D3-3	C-1	E10-10

Table 5-2 (Cont)
LPSKW Data: DZLPD, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
KWT31				
	LOAD BUF H	D3-1	C-1	E34-13
	COUNT L	D3-1	C-1	E43-5
	10KHZ L	D3-1	B-3	E30-13
	RATE 0 (1) H	D3-3	C-1	E10-14
	RATE 1 (1) H	D3-3	C-1	E10-10
KWT32				
	LOAD BUF H	D3-1	C-1	E34-13
	COUNT L	D3-1	C-1	E43-5
	1KHZ L	D3-1	B-3	E36-13
	RATE 2 (1) H	D3-1	C-1	E10-7
KWT33				
	COUNT L	D3-1	C-1	E43-5
	100HZ L	D3-1	B-2	E42-13
	RATE 0 (1) H	D3-1	C-1	E10-14
	RATE 2 (1) H	D3-1	C-1	E10-7
	LOAD BUF H	D3-1	C-1	E34-13
KWT34				
	COUNT L	D3-1	C-1	E43-5
	ST PULSE (1) L	D3-1	C-4	E41-6
	RATE 1 (1) H	D3-3	C-2	E10-10
	RATE 2 (1) H	D3-3	C-2	E10-7
	LOAD BUF H	D3-1	C-1	E34-13
KWT35				
	MODE 00 (1) H	D3-3	D-1	E5-15
	MODE 01 (1) H	D3-3	D-1	E5-10
	COUNT L	D3-1	C-1	E45-5
	RATE 0 (1) H	D3-3	C-2	E10-15
	LOAD BUF H	D3-1	C-1	E34-13
	CKBF (1) L	D3-1	C-3	E28-6
KWT36				
	B INIT L	D3-1	D-7	E38-8
	RATE 0 (1) H	D3-3	C-2	E10-15
	RATE 1 (1) H	D3-3	C-2	E10-10
	RATE 2 (1) H	D3-3	C-2	E10-7
KWT37				
	B INIT L	D3-1	D-7	E38-8
	MODE 00 (1) H	D3-3	D-2	E5-15
	MODE 01 (1) H	D3-3	D-2	E5-10

Table 5-2 (Cont)
LPSKW Data: DZLPD, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
KWT38				
	B INIT L	D3-1	D-7	E38-8
	FLAG 2 (1) H	D3-3	B-5	E21-5
	INT ENA 2 (1) L	D3-3	D-2	E5-3
	ST ENA (1) H	D3-3	D-2	E5-7
KWT39				
	B INIT L	D3-1	D-7	E38-8
	FLAG 1 (1) H	D3-3	A-4	E21-9
	INT ENA 1 (1) L	D3-3	C-2	E10-3
KWT40				
	B INIT L	D3-1	D-7	E38-8
	ENA CT (1)	D3-3	B-1	E26-9
KWT41				
	COUNT L	D3-1	C-1	E43-5
	1 MHZ L	D3-1	B-4	E25-14
	MODE 00 + 01	D3-3	D-1	
	A OV L	D3-2	D-7	E6-12
	OV LD (1) H	D3-1	A-4	E39-5
	ENA CT (1) H	D3-3	B-1	E26-9
KWT42				
	COUNT L	D3-1	C-1	E43-5
	100KHZ L	D3-1	B-4	E25-13
	MODE 00 + 01	D3-3	D-1	
	A OV L	D3-2	D-7	E6-12
	OV LD (1) H	D3-1	A-4	E39-5
	ENA CT (1) H	D3-3	B-1	E26-9
	FLAG 1 (1) H	D3-3	A-5	E21-9
KWT43				
	COUNT L	D3-1	C-1	E43-5
	10KHZ L	D3-1	B-3	E30-13
	A OV L	D3-2	D-7	E6-12
	OV LD (1) H	D3-1	A-4	E39-5
	FLAG 1 (1) H	D3-3	A-5	E21-9
KWT44				
	COUNT L	D3-1	C-1	E43-5
	1KHZ L	D3-1	B-3	E36-13
	A OV L	D3-2	D-7	E6-12
	OV LD (1) H	D3-1	A-4	E39-5
	FLAG 1 (1) H	D3-3	A-5	E21-9

Table 5-2 (Cont)
LPSKW Data: DZLPD, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
KWT45				
	COUNT L	D3-1	B-1	E43-5
	100HZ L	D3-1	B-2	E42-13
	OV LD (1) H	D3-1	A-4	E39-5
	FLAG 1 (1) H	D3-3	A-5	E21-9
KWT46				
	COUNT L	D3-1	B-1	E43-5
	LTC	D3-1	D-6	E44-3
	CLK IN L	D3-1	D-5	E44-8
	OV LD (1) H	D3-1	A-4	E39-5
	FLAG 1 (1) H	D3-3	A-5	E21-9
KWT47				
	COUNT L	D3-1	B-1	E43-5
	ENA CT (1) H	D3-3	B-1	E26-9
	OV LD (1) H	D3-1	A-4	E39-5
KWT48				
	COUNT L	D3-1	B-1	E43-5
	ENA CT (1) H	D3-3	B-1	E26-9
	OV LD (1) H	D3-1	A-4	E39-5
KWT49				
	INT B H	D3-3		E26-6
	REFER TO DMA OPTION			
KWT50				
	INT B H	D3-3	A-4	E26-6
	INT DONE B H	D1-4	A-5	E22-6
	REFER TO DMA OPTION			
KWT51				
	LOAD BUF H	D3-1	C-1	E34-13
	COUNT L	D3-1	B-1	E43-5
	OV LD (1) H	D3-1	A-4	E39-5
	INT B H	D3-3	A-4	E26-6
KWT52				
	INT ENA 1 (1) L	D3-3	C-1	E10-3
	INT B H	D3-3	A-4	E26-6
KWT53				
	INT ENA 1 (1) L	D3-3	C-1	E10-3
	INT B H	D3-3	A-4	E26-6
	REFER TO DMA OPTION			

Table 5-2 (Cont)
LPSKW Data: DZLPD, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
KWT54				
	INT ENA 1 (1) L	D3-3	C-1	E10-3
	INT B H	D3-3	A-4	E26-6
	REFER TO DMA OPTION			
KWT55–KWT62				
	COUNT L	D3-1	B-1	E43-5
	A OV L	D3-2	D-8	E6-12
	COUNTER REG	D3-2	BCD-8	

Table 5-3
LPSDR Data: DZLPD, Test B

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
DRT0				
	LD OUT LOW H	D4-3	D-2	E25-11
	LD OUT HIGH H	D4-3	D-2	E25-8
	OUTPUT REGISTER	D4-3	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	
DRT1				
	B INIT L	D4-2	B-4	E22-10
	OUTPUT REGISTER	D4-3	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	
DRT2–DRT3				
	LD OUT LOW H	D4-3	D-2	E25-11
	LD OUT HIGH H	D4-3	D-2	E25-8
	OUTPUT REGISTER	D4-3	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	
DRT4				
	LD OUT LOW H	D4-3	D-2	E25-11
	OUTPUT REGISTER	D4-3	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	
DRT5				
	LD OUT HIGH H	D4-2	D-2	E25-8
	OUTPUT REGISTER	D4-2	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	

Table 5-3 (Cont)
LPSDR Data: DZLPD, Test B

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
DRT6				
	LD OUT LOW H	D4-3	D-2	E25-11
	OUTPUT REGISTER	D4-3	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	
DRT7				
	LD OUT HIGH H	D4-3	D-2	E25-11
	OUTPUT REGISTER	D4-2	ABCD-6	
	READ OUTPUT L	D4-2	B-4	E19-6
	OUTPUT MUX	D4-1	ABCD-4	
DRT8				
	SB 00 (1) H	D4-2	C-3	E27-5
	LD STATUS LOW H	D4-2	C-4	E25-6
	RD STATUS H	D4-2	D-6	E14-12
DRT9				
	SB 08 (1) H	D4-2	D-3	E24-9
	LD STATUS HIGH H	D4-2	C-4	E25-6
	RD STATUS H	D4-2	D-6	E14-12
DRT10				
	OUT FLAG (1) H	D4-2	D-5	E29-5
DRT11				
	SB 14 (1) H	D4-2	D-3	E24-5
DRT12				
	IN FLAG (1) H	D4-2	D-6	E30-5
DRT13				
	SB 06 (1) H	D4-2	C-3	E27-9
	IBUS DATA 06 L	D4-2	D-1	E20-13
DRT14				
	INIT L	D4-2	A-5	E22-10
	OUT FLAG (1) H	D4-2	D-5	E29-5
	SB 14 (1) H	D4-2	D-3	E24-5
	SB 08 (1) H	D4-2	D-3	E24-9
	IN FLAG (1) H	D4-2	C-6	E30-5
	SB 06 (1) H	D4-2	C-3	E27-9
	SB 00 (1) H	D4-2	C-3	E27-5

Table 5-3 (Cont)
LPSDR Data: DZLPD, Test B

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
DRT15–DRT18				
	I/O Test cable must be connected			
	IN LD H	D4-1	A-7	E21-6
	INPUT REGISTER	D4-1	ABCD-6	
	READ INPUT L	D4-2	B-5	E19-3
	DATA MUX	D4-1	ABCD-4	
DRT19				
	IN FLAG (1) H	D4-2	C-6	E30-5
	EXT NEW DATA READY L	D4-2	D-7	E30-4
DRT20				
	OUT FLAG (1) H	D4-2	D-5	E29-5
	EXT DATA ACCEPT L	D4-2	D-6	E29-4
DRT21				
	IN FLAG (1) H	D4-2	C-6	E30-5
	INT C H	D4-2	C-5	E30-9
	OUT FLAG (1) H	D4-2	D-5	E29-5
	INT D H	D4-2	B-7	E29-9
DRT22				
	INT C H	D4-2	C-5	E30-9
DRT25				
	INT D H	D4-2	A-7	E29-9
DRT29–DRT30				
	INT C H	D4-2	C-5	E30-9
	INT D H	D4-2	B-7	E29-9
	SB 14 (1) H	D4-2	D-3	E24-5
	SB 06 (1) H	D4-2	C-3	E27-9

Table 5-4
LPSVC Data: DZLPD, Test C

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
VCT1				
	INIT L	D10-2	A-4	E13-10
	DONE (1) H	D10-2	C-4	E8-5
	IBUS D07	D10-2	C-7	E23-4
	RD STATUS L	D10-1	B-5	E3-6
	No other status bit should be set			

Table 5-4 (Cont)
LPSVC Data: DZLPD, Test C

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
VCT1				
	LD STATUS LB H	D10-1	A-6	E12-8
	FAST INTENSE (1) H	D10-1	A-5	E11-10
	RD STATUS L	D10-2	B-5	E3-6
	IBUS D01 L	D10-1	A-7	E17-1
VCT2				
	LD STATUS LB H	D10-1	A-6	E12-8
	MODE 0 (1) H	D10-1	A-5	E11-15
	RD STATUS L	D10-2	B-5	E3-6
	IBUS D02 L	D10-1	B-7	E17-4
VCT3				
	LD STATUS LB H	D10-1	A-6	E12-8
	MODE 1 (1) H	D10-1	A-5	E11-7
	RD STATUS L	D10-2	B-5	E3-6
	IBUS D03 L	D10-1	B-7	E17-13
VCT4				
	LD STATUS HB H	D10-1	B-5	E12-3
	EXT DEL (1) H	D10-1	B-1	E18-8
	RD STATUS L	D10-2	B-5	E3-6
	IBUS D04 L	D10-1	B-7	E17-10
VCT5				
	LD STATUS LB H	D10-1	B-5	E12-8
	INT EN (1) H	D10-1	A-5	E11-2
	RD STATUS L	D10-1	B-5	E3-6
	IBUS D06 L	D10-2	B-7	E23-1
VCT6				
	LD STATUS HB H	D10-1	B-5	E12-3
	CHANNEL 2 H	D10-1	A-3	E28-7
	RD STATUS L	D10-1	B-5	E3-6
	IBUS D09 L	D10-2	C-7	E30-12
VCT7				
	LD STATUS HB H	D10-1	B-5	E12-3
	STORE H	D10-1	A-4	E28-2
	RD STATUS L	D10-1	B-5	E3-6
	IBUS D10 L	D10-2	D-7	E30-10
VCT8				
	LD STATUS HB H	D10-1	B-5	E12-3
	NOT WRITE THRU H	D10-1	A-4	E28-15
	RD STATUS L	D10-1	B-5	E3-6
	IBUS D11 L	D10-2	D-7	E23-13

Table 5-4 (Cont)
LPSVC Data: DZLPD, Test C

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
VCT9–VCT12				
	LD X L	D10-1	D-5	E12-6
	X REGISTER	A625	BCD-6	
	RD X L	D10-1	D-5	E3-8
	X-Y OUTPUT MUX	A625	BCD-2	
VCT13–VCT16				
	LD Y L	D10-1	C-5	E12-11
	Y REGISTER	A625	BCD-4	
	RD Y L	D10-2	C-5	E3-3
	X-Y OUTPUT MUX	A625	BCD-2	
VCT17				
	LD X L	D10-1	D-5	E12-6
	LD Y L	D10-1	C-5	E12-11
	X REGISTER	A625	BCD-6	
	Y REGISTER	A625	BCD-4	
	X-Y OUTPUT MUX	A625	BCD-2	
	RD X L	D10-1	D-5	E3-8
	RD Y L	D10-1	C-5	E3-3
VCTST2				
	FAST INTENSE (0) H	D10-1	A-5	E11-11
	DONE (1) H	D10-2	C-3	E8-5
	START DEL H	D10-2	D-5	E25-8
	INTEN PULSE H	D10-2	D-2	E14-8
VCTST3 & VCTST4				
	RED H	D10-1	A-4	E28-10
	RED DELAY H	D10-2	B-4	E21-5
	LD STATUS HB H	D10-1	B-5	E12-3
	COLOR PL H	D10-2	B-3	E6-5
	DONE (1) H	D10-2	C-3	E8-5
VCTST5 & VCTST6				
	GREEN H	D10-1	A-4	E28-11
	GREEN DELAY H	D10-2	A-4	E6-13
	LD STATUS HB H	D10-1	B-5	E12-3
	COLOR PL H	D10-2	B-3	E6-5
	DONE (1) H	D10-2	C-3	E8-5
VCTST7 & VCTST8				
	MODE 0 (1) H	D10-1	A-5	E11-15
	LD STATUS LB H	D10-1	B-5	E12-8
	LD X L	D10-1	D-5	E12-6
	DONE (1) H	D10-2	C-3	E8-5
	START DEL H	D10-2	D-5	E25-8
	INTEN PULSE H	D10-2	D-2	E14-8

Table 5-4 (Cont)
LPSVC Data: DZLPD, Test C

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
VCTST9 & VCTST10				
	MODE 1 (1) H	D10-1	A-5	E11-7
	LD STATUS LB H	D10-1	B-5	E12-8
	LD Y L	D10-1	C-5	E12-11
	DONE (1) H	D10-2	C-3	E8-5
	START DEL H	D10-2	D-5	E25-8
	INTEN PULSE H	D10-2	D-2	E14-8
VCTS11				
	ERASE (1) H	D10-1	B-2	E18-5
	DONE (1) H	D10-2	C-3	E8-5
	ERASE CLEAR H	D10-2	C-6	E13-9
VCTS12–VCTS15				
	FAST INTENSE (1) H	D10-1	A-5	E11-10
	START DEL H	D10-2	D-5	E25-8
	INTEN PULSE H	D10-2	D-2	E14-8
	DONE (1) H	D10-2	C-3	E8-5

Table 5-5
LPSAD-12 Data: DZLPC, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
ADTST0				
	INT ENA (1) H	D2-2	B-2	E16-5
	INT A H	D2-1	A-2	E35-8
	INT L	D2-4	C-6	E36-10
	I BUS ENABLE RT L	D2-4	A-3	F
ADT1				
	SEL 0 (1)	D2-2	B-5	E32-2
	I BUS D01	D2-3	A-3	E15-4
	STATUS IN L	D2-4	B-6	E35-3
	LD STATUS LOW H	D2-2	A-7	E28-3
ADT2				
	SEL L (1) H	D2-2	B-5	E32-7
	I BUS D02 L	D2-3	B-3	E15-12
ADT3				
	BURST MODE (1) H	D2-2	B-5	E32-10
	I BUS D03 L	D2-3	B-3	E15-13
ADT4				
	STT ENA (1) H	D2-2	B-5	E32-15
	I BUS D04 L	D2-3	B-3	E19-3

Table 5-5 (Cont)
LPSAD-12 Data: DZLPC, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
ADT5				
	OV ENA (1) H	D2-2	B-2	E16-9
	I BUS D05 L	D2-3	B-3	E19-4
	LO STATUS LOW H	D2-2	A-7	E28-3
ADT6				
	INT ENA (1) H	D2-2	B-2	E16-5
	I BUS D06 L	D2-3	B-3	E19-12
ADT7				
	MUX 0 (1) H	D2-2	C-5	E2-2
	I BUS D08 L	D2-3	C-3	E6-3
	LD STATUS HIGH H	D2-2	C-7	E28-11
ADT10				
	MUX (1) H	D2-2	C-5	E2-7
	I BUS D09 L	D2-3	C-3	E6-4
ADT11				
	MUX 2 (1) H	D2-2	C-3	E2-10
	I BUS D10 L	D2-3	C-3	E6-12
ADT12				
	MUX 3 (1) H	D2-2	C-5	E2-15
	I BUS D11 L	D2-3	C-3	E6-13
ADT13				
	MUX 4 (1) H	D2-2	C-5	E3-2
	I BUS D12 L	D2-3	D-3	E11-3
ADT14				
	MUX 5 (1) H	D2-2	D-5	E3-7
	I BUS D13 L	D2-3	D-3	E11-4
ADT15				
	DUAL ENA (1) H	D2-2	D-5	E3-10
	I BUS D14 L	D2-3	D-3	E11-12
ADT16				
	ERR (1) H	D2-1	B-3	E21-8
	I BUS D15 L	D2-3	D-3	E11-13
ADT17				
	ST 00 (1) H	D2-1	D-2	E21-5
	HOLD (1) H	D2-1	C-4	E14-6
	PST (1) H (DLY)	D2-1	C-5	E39-13
	I BUS D00 L	D2-3	A-3	E15-3

Table 5-5 (Cont)
LPSAD-12 Data: DZLPC, Test A

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
ADT20				
	ST 00 (1) H	D2-1	D-2	E21-5
	EOC L	D2-1	B-7	E22-1
	DONE (1) H	D2-1	B-5	E26-9
ADT21				
	ST 00 (1) H	D2-1	D-2	E21-5
	ERR (1) H	D2-1	B-4	E21-8
	STP L	D2-1	D-7	E09-13
ADT22				
	STT ENA (1) H	D2-2	B-5	E32-15
	HOLD (1) H	D2-1	D-4	E14-6
	ST 00 (1) H	D2-1	D-2	E21-5
ADT23				
	OV ENA (1) H	D2-2	B-2	E16-9
	OVERFLOW L	D2-1	D-6	E10-6
	STT ENA (1) H	D2-2	B-5	E32-15
ADT24–ADT26				
	INT A H	D2-1	A-3	E35-8
	DONE (1) H	D2-1	B-5	E26-9
ADT27				
	MUX 0–5	D2-2	CD-5	
	B INIT L	D2-4	C-6	E36-10
ADT30				
	OV ENA (1) H	D2-2	B-2	E16-9
	INT ENA (1) H	D2-2	B-2	E16-5
	STT ENA (1) H	D2-2	B-5	E32-15
	B INIT L	D2-4	C-6	E36-10
ADT31				
	DONE (1) H	D2-1	B-5	E26-9
	ERR (1) H	D2-1	B-3	E21-8
	B INIT L	D2-4	C-6	E36-10
ADT32				
	SEL 0 (1) H	D2-2	B-2	E32-2
	SEL 1 (1) H	D2-2	B-2	E32-7
	BURST MODE (1) H	D2-2	B-2	E32-10
	B INIT L	D2-4	C-6	E36-10

Table 5-6
LPSAD-NP Data: DZLPC, Test B

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
DMAT0–DMAT3				
	CURRENT ADDRESS REGISTER	D9-3		
	LD CA L	D9-1	B-6	E33-4
	RD CA L	D9-1	B-6	E33-12
	OUTPUT MUX	D9-4	MBCD-3	
DMAT4-DMAT7				
	WORD COUNT REGISTER	D9-4	ABCD-6	
	LD WC L	D9-1	B-5	E33-5
	RD WC L	D9-1	B-5	E33-11
	OUTPUT MUX	D9-4	ABCD-3	
DMAT10				
	DMA (1) H	D9-1	B-2	E29-9
	LD STATUS H	D9-1	B-6	E27-8
	RD WC L	D9-1	B-5	E33-11
	OUTPUT MUX	D9-4	ABCD-3	
DMAT11				
	LD STATUS H	D9-1	B-6	E27-8
	XCA 16 H	D9-3	C-7	E32-3
	RD WC L	D9-1	B-5	E33-11
	OUTPUT MUX	D9-4	ABCD-3	
DMAT12				
	LD STATUS H	D9-1	B-6	E27-8
	XCA 17 H	D9-3	C-7	E32-2
	RD WC L	D9-1	B-5	E33-11
	OUTPUT MUX	D9-1	ABCD-3	
DMAT13				
	CURRENT ADDRESS REGISTER	D9-3		
	B INIT L	D9-1	A-6	E27-6
	OUTPUT MUX	D9-4		
	RD CA L	D9-1	B-6	E33-12
DMAT14				
	WORD COUNT REGISTER	D9-4		
	B INIT L	D9-1	A-6	E27-6
	OUTPUT MUX	D9-4		
	RD WC L	D9-1	B-5	E33-11
DMAT15				
	DMA (1) H	D9-1	B-2	E29-8
	B INIT L	D9-1	A-6	E27-6

Table 5-6 (Cont)
LPSAD-NP Data: DZLPC, Test B

Subtest	Signal Mnemonic	Drawing	Coordinates	IC Pin
DMAT16				
	DMA (1) H	D9-1	B-2	E29-9
	REFER TO A/D LOGIC			
DMAT17–20				
	CA REGISTER	D9-3		
	WC REGISTER	D9-4		
	BUS ADDRESS DRIVERS	D9-3		
	END CYCLE H (CA)	D9-2	B-7	E11-4
	NPR REQ (1) L (WC)	D9-1	D-6	E29-5
DMAT21				
	TIME OUT (1) H	D9-2	C-3	E6-9

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CHANGE DOCUMENT
LPS11-S LABORATORY PERIPHERAL SYSTEM MAINTENANCE MANUAL
DEC-11-HLPMA-B-D
JUNE 1974

This change document contains new and revised pages to update the LPS11-S Maintenance Manual to include the LPSAM-SG and BA408 Switched Gain options. Replace the existing pages with the revised pages and add the new pages.

Pages:
iii, iv
v, vi
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3-26, blank
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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

LTC:

Frequency:	ac line 50/60 Hz
Output – High Voltage:	2.4V minimum 3.3V typical
Output – Low Voltage:	0.4V maximum 0.2V typical @ 16 mA

AC LOW and DC LOW:

Output – High Voltage:	3.5V minimum
Output – Low Voltage:	0.8V maximum @ 50 mA

1.4.8 LPSAM-SG/BA408 Switched Gain Multiplexer

Electrical

Input Channels	8 (single-ended)
Switching	Break-before-make
Input Range	±5 V G=1 ±1.25 V G=4 ±312.5 mV G=16 ±78.125 mV G=64
Gain Accuracy	0.02%
Linearity	0.01%
Input Impedance	10^9 in parallel with 0.01 μF
Input Bias Current	±400 nA max., $-15\ V \leqslant V_{in} \leqslant +10\ V$
Input Offset Voltage	Adjustable to zero
Offset Drift	5 μV/° C max. RTI* + 120 μV/° C max. RTO*
Bandwidth	100 kHz min., 150 kHz typ.
Settling Time (to ±½ LSB)	15 μs max.
Crosstalk	80 db min. at 1 kHz, 20 db/decade rolloff
Noise (rms)	70 μV max. RTI* + 550 μV max. RTO*
Warmup Time	3 minutes

*RTI = referred to input
*RTO = referred to output

Power Requirements

+15 V ± 0.1% at 65 mA max.
-15 V ± 0.1% at 40 mA max.
+5 V ± 5% at 120 mA max.

Environmental

Operating Temperature	40° – 110° F (4° – 43° C)
Operating Humidity	20% – 80% non-condensing
Storage Temperature	0° – 125° F (-18° – 57° C)
Storage Humidity	5% – 95% non-condensing

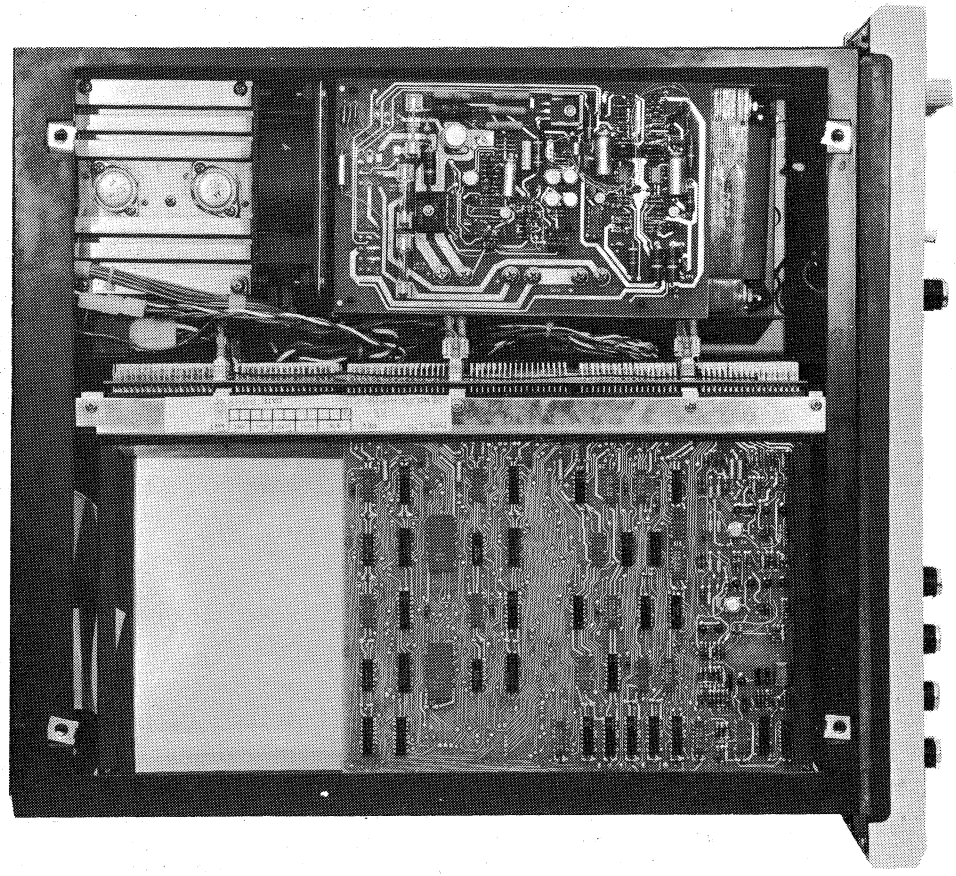

Figure 2-2 LPS11-S with Top Cover Removed

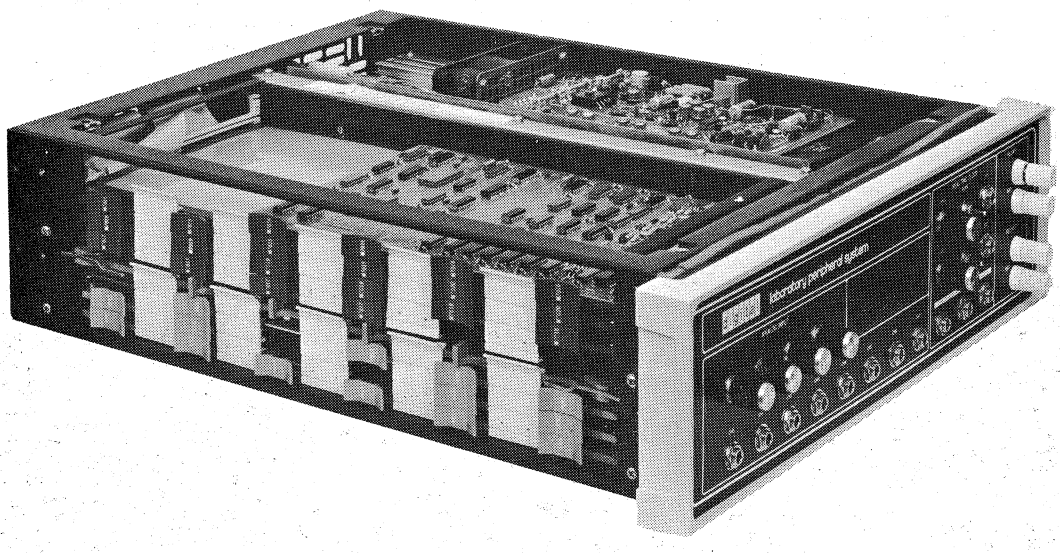

Figure 2-3 LPS11-S Mounting Box with Top Cover and Side Panel Removed

Figure 2-4 shows the mounting box complete with modules, together with a guide illustrating the option slot allocations. Module guides assist in inserting the modules into the proper slots.

Figure 2-5 is a rear view of the mounting box. An ON/OFF power switch is provided for maintenance purposes. The power control circuit breaker protects the power supply from overload.

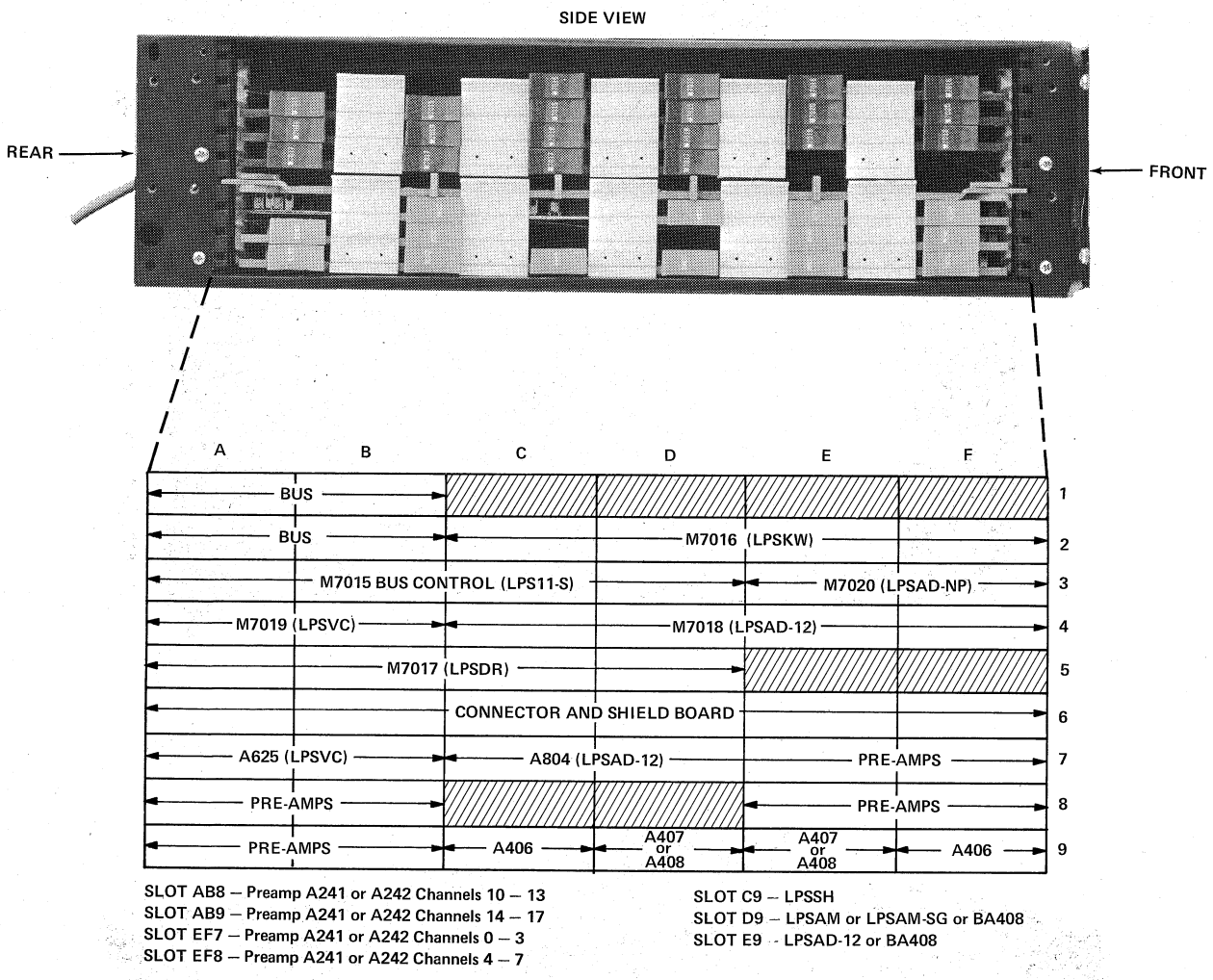

Figure 2-4 LPS11-S Option Slot Allocations

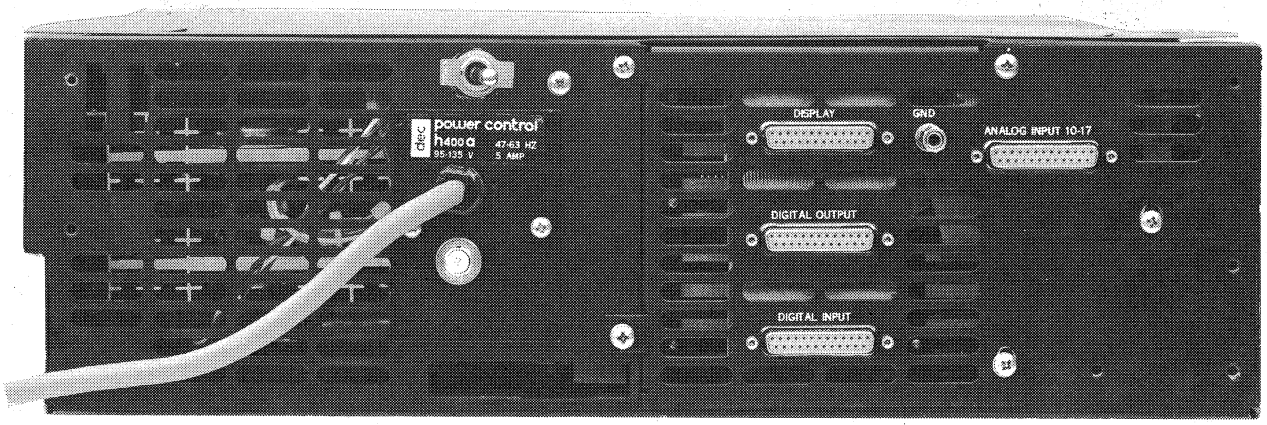

Figure 2-5 LPS11-S Rear View

4. Insert the bus control module (M7015) into slots A3/B3/C3/D3 (Figure 2-4).

5. Insert the digital I/O module (M7017) into slots A5/B5/C5/D5.

6. Remove the screws securing the rear connector panel and open the panel as far as cable lead length will allow.

7. Remove modules as required to permit access to the connector panel.

8. Attach the longer of the two cable connectors (using the hardware supplied) to the DIGITAL OUTPUT slot. Connect the shorter cable connector to the DIGITAL INPUT slot.

9. Route both cables through card guide assembly between slots 5 and 6.

10. Connect the cables to their respective input and output connectors designated D I/O INPUT and D I/O OUTPUT, respectively, on the M996 module.

11. Replace the modules removed in step 7.

12. Replace the rear connector panel and secure the Unibus cable.

13. Insert the two identical relays into the relay sockets located on the inside of the front panel. Attach the relay retaining clips to secure the relays in place.

14. Replace the top cover and side panel of the LPS11-S.

15. Conduct an acceptance test as described in the LPS11-S Acceptance Procedures (A-SP-LPS11-S-14) to ensure that the LPSDR Digital Input/Output option is installed properly and operating correctly.

2.9.10 BA408 Switched Gain Multiplexer (Channels 0–7)

The BA408 Switched Gain Multiplexer option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.

2. Remove the H755 power supply from the LPS11-S.

3. Remove the A407 Fixed Gain Multiplexer module from slot E09.

4. Install ECOs on A/D Control Board M7018 and backpanel as described in the *LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure* (A-SP-LPSAM-SG-2).

5. Check that W2 is in the "0–7" position on the A408 module.

6. Insert the A408 module into slot E09.

7. Install the magnetic shield in the H755 as shown in the H755 print set (E-UA-H755-0-0).

8. Replace the H755 in the LPS11-S.

9. Conduct an acceptance test as described in the LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure to ensure that the BA408 Switched Gain Multiplexer option is installed properly and operating correctly.

10. Install the top cover and side panel of the LPS11-S.

2.9.11 LPSAM-SG Switched Gain Multiplexer (Channels 10–17)

The LPSAM-SG Switched Gain Multiplexer option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.
2. Ensure that a BA408 option has already been installed in channels 0–7 per Paragraph 2.9.10. (Switched gain and fixed gain multiplexers may not be mixed.)
3. Check that W2 is in the "10–17" position on the A408 Switched Gain Multiplexer.
4. Insert the Switched Gain Multiplexer module into slot D09 (Figure 2-4).
5. Attach the extender handles to the end of the G728 jumper modules.
6. Insert one of the jumper modules into slot A8/B8 and the other into slot A9/B9.
7. Remove the screws securing the rear connector panel to the mounting box; open the panel as far as the cable lead length will allow.
8. Remove modules as required to permit access to the connector panel. Attach the cable assembly (using the hardware supplied) to the ANALOG INPUT 10–17 slot.
9. Route the cable through the card guide assembly between slots 5 and 6 and insert the connector into the A/D 10–17 connector on the M996 Connector Shield Board.
10. Replace all of the modules removed in step 7.
11. Replace the rear connector panel and secure the Unibus cable as described in Paragraph 2.8.
12. Conduct an acceptance test as described in the LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure (A-SP-LPSAM-SG-2) to ensure that the LPSAM-SG 10–17 Switched Gain Multiplexer channels 10–17 option is installed properly and operating correctly.
13. Replace the top cover and side panel of the LPS11-S.

2.9.12 BA408 Switched Gain Multiplexer (Channels 10–17)

The BA408 Switched Gain Multiplexer option is installed in the following manner:

1. Remove the top cover and side panel of the LPS11-S.
2. Remove the fixed gain MUX A407 from slot D09.
3. Ensure that a BA408 option has already been installed in channels 0–7 per Paragraph 2.9.10. (Switched gain and fixed gain multiplexers may not be mixed.)
4. Check that W2 is in the "10–17" position on the A408 module.
5. Insert the A408 module into slot D09.
6. Conduct an acceptance test as described in the LPSAM-SG/BA408 Installation/Checkout/Acceptance Procedure, to ensure that the BA408 Switched Gain Multiplexer option is installed properly and operating correctly.
7. Install the top cover and side panel of the LPS11-S.

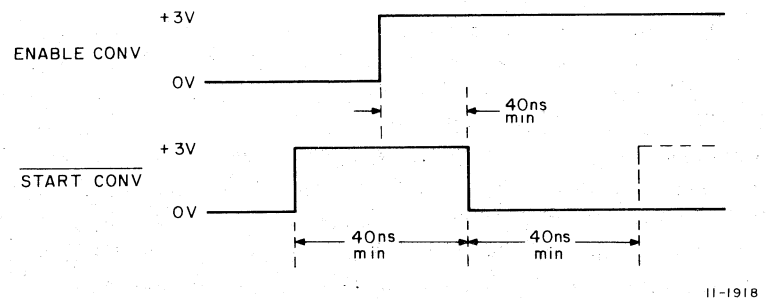

Figure 3-23 A804 Timing Requirements

If ENABLE CONV goes high while $\overline{\text{START CONV}}$ is low, a conversion will also be initiated. The actual conversion is delayed 200 ns to ensure adequate time for the clock to reset. The CONV output goes high within 65 ns and $\overline{\text{CONV}}$ goes low within 80 ns of the $\overline{\text{START CONV}}$ initiation transition. Both CONV and $\overline{\text{CONV}}$ remain asserted during conversion, and terminate at the end of conversion.

The sequencer is a 12-bit shift register through which one "0" is shifted from the MSB to each bit in sequence. The sequencer outputs are ORed with each of the corresponding holding register outputs to the D/A converter inputs. The sequencer interrogates each D/A bit in order, starting with the MSB. At the end of each interrogation, the holding register is clocked to accept or reject the bit. That decision is arrived at by summing the currents of the D/A converter output and the analog input, which are of opposite polarity, so that the current sum actually represents the difference between the two. The voltage resulting from a current imbalance is fed into a voltage comparator referenced to common, and the output of the comparator is tied back to the common DATA line of the holding register. If the interrogated D/A bit supplies more current than the analog input removes, the result is a positive voltage and the bit is rejected; i.e., "0." If the result is a negative voltage, the bit is set to "1." In this way, the converter zeroes in on the correct value, providing a more accurate approximation with each successive decision.

The PC rotary switch connects the last desired bit of the sequencer to the clock input of the CONV status flip-flop and the data input of clock control flip-flop. When the connected bit interrogation terminates, the decision is clocked into the holding register, the clock is inhibited, the CONV status flip-flop is complemented, and the sequencer is loaded with all "1s," indicating the end of the conversion.

A special strobe circuit connected to the output of the comparator allows the comparator decision to be available for only 100 ns, preventing stray feedback from propagating through and affecting the final result.

3.2.10.5 A408 Switched Gain Multiplexer – The A408 contains a single multiplexer and programmable gain amplifier which provide 8 channels and 4 different gains (1, 4, 16, 64) to process analog input signals. This 8-channel capacity can be extended to 16 channels by the addition of a second 8-channel switched gain multiplexer (LPSAM-SG). When using the A408s in place of the A407s, the 16 channels which make up the LPSAD-12 will be designated as follows:

Address	Result
Channels 0–17	Channels 0–17 at G=1
Channels 20–37	Channels 0–17 at G=4
Channels 40–57	Channels 0–17 at G=16
Channels 60–77	Channels 0–17 at G=64

Multiplexer selection is determined by attaching W2 in the appropriate position ("0–7" or "10–17"). Channel selection is determined by the four MUX signals, MUX 0 L, MUX 1 L, MUX 2 L, and MUX 3 L. If the module is to be used for channels 0–7, W2 is left in the "0–7" position, so that MUX 3 L is applied directly to pin 1 of the multiplexer chip, IC E1, thereby enabling the multiplexer when MUX 3 is in the 0 state, i.e., MUX 3 L is high (pulled up to +10 V). If the module is to be used for channels 10–17, W2 is moved to the "10–17" position, so that the inverted MUX 3 L is applied to pin 1 of the multiplexer chip, thereby enabling the multiplexer when MUX 3 is in the 1 state, i.e., MUX 3 L is low. MUX 0 L, MUX 1 L and MUX 3 L are applied directly to the multiplexer chip to select the desired channel. The low input on these three lines is ground at the module's input pin, clamped by D50, D51 or D52, to +4 V at the multiplexer chip input. If all three are low, channel 7 is enabled; if all three are high (pulled up to +10 V), channel 0 is enabled.

Gain level (1, 4, 16 or 64) is determined by the state of MUX 4 L and MUX 5 L. If MUX 4 L and MUX 5 L are both high (0,0) at the pin 12 and 13 inputs of E5, then E5 pin 11 is low, selecting a gain of 1. If MUX 4 L and MUX 5 L are both low (1,1), high levels result at the pin 1 and 2 inputs of E5, so that E5 pin 3 is low, selecting a gain of 64.

The RTO fine (R24) and RTO coarse (R25) pots are used to adjust for zero at the output of E3 at a gain of 1.

The RTI circuit, consisting of Q3, Q2, R22 and associated components, is used to adjust for zero at the output of E3 at a gain of 64.

E2 and E6 are 1-of-4 multiplexers. E2 is used to select the correct resistor value to maintain the amplifier bandwidth constant at the different gains. E6 is used to select the correct voltage level to be fed back to the input of E3. The feedback ratios for the 4 different gains are determined by the resistor divider network consisting of R37–R42.

Each of the analog input channels contains a 47-ohm fusible resistor and two clamping diodes, which provide over-voltage protection for the multiplexer circuits.

3.2.11 Direct Memory Access (DMA)

The LPSAD-NP DMA option is used only in conjunction with the LPSAD-12. DMA adds additional speed to the A/D conversion process by storing A/D conversions in memory without program intervention. The LPSAD-12 and LPSAD-NP can operate in four modes of operation: single conversion, dual sample-and-hold, single burst, or dual sample-and-hold burst modes.

3.2.11.1 DMA Programming – A/D Status register bits 02 and 01 are used to point to the DMA registers (Figure 3-24), which consist of Status, Word Count, and Current Address registers with associated control and timing circuits.

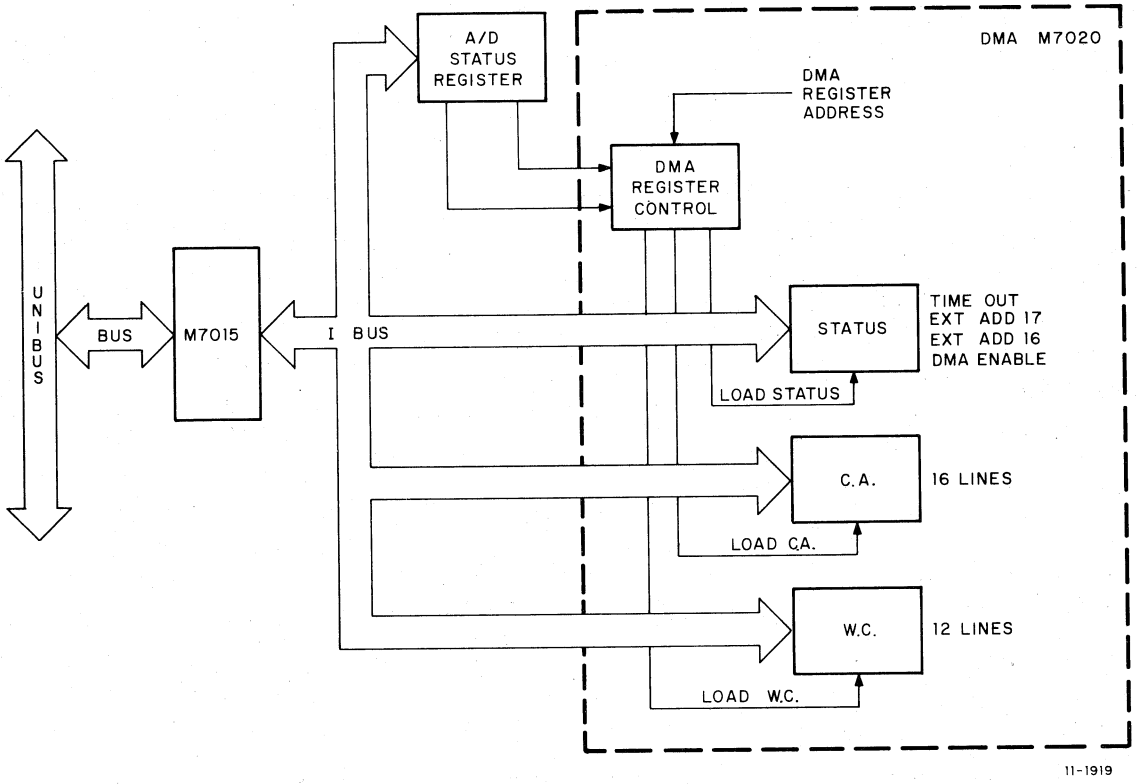

Figure 3-24 DMA Register Control Block Diagram

To address the DMA registers, it is first necessary to address the A/D Status register and supply the proper bit configuration for bits 02 and 01, (as shown in Figure 3-25 and described in Table 3-10), after which the DMA Status register may be addressed (Figure 3-26 and Table 3-11).

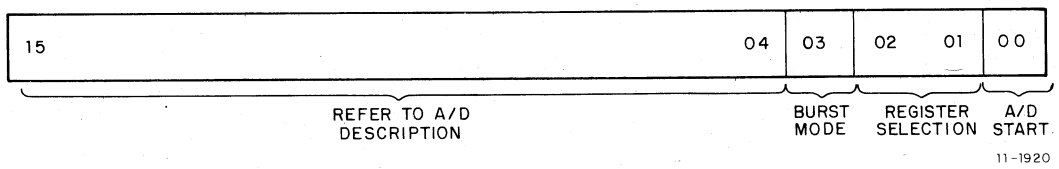

Figure 3-25 A/D Status Register DMA Bit Assignments

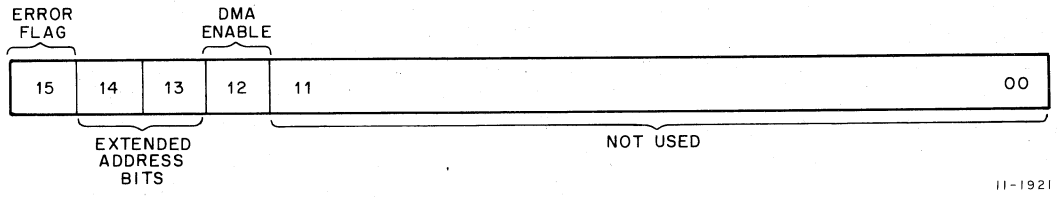

Figure 3-26 DMA Status Register Bit Assignments

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4.2.3 Single Sample-and-Hold System Calibration

The calibration procedure for single sample-and-hold systems is as follows:

1. Connect EDC output to channel 0 input.

2. Load system diagnostic and select calibration test (C). Select channel 0 by leaving Switch register at 000000_8.

3. With EDC voltage set per line A of Table 4-9, adjust A406 Sample-and-Hold module potentiometer R27 (right-hand side) to obtain, as nearly as possible, the 0000-to-0001 transition as viewed on the LED display.

4. Adjust A804 A/D Converter module potentiometer R16 (right-hand side) for the exact point of 0000-to-0001 transition (50-50 duty cycle).

NOTE

It is important to get as close as possible to the 0000-to-0001 transition point with the A407 potentiometer (R27) before trimming up with the A804 potentiometer (R16) to minimize subsequent temperature drift. In no instance should it be necessary to take out more than one or two counts using A804 potentiometer R16.

5. Set the EDC voltage as indicated on line B of Table 4-9, and adjust A804 potentiometer R15 (left-hand side) for the exact point of the 7776-to-7777 transition (50-50 duty cycle). Recheck the adjustments of steps 3 through 5, if necessary.

Table 4-9
Sample-and-Hold System Calibration Data

Test	Input Voltage		Adjustment Potentiometers	Transition Point Viewed on LED Display
	With LPSAG Preamps	Without LPSAG Preamps		
A	-0.99975V	-4.99875V	A406: R27 A804: R16	0000/0001
B	+0.99925V	+4.99625V	A804: R15	7776/7777

4.2.4 Dual Sample-and-Hold System Calibration

The LPSSH option provides a dual sample-and-hold capability for the LPS11-S analog system. The system calibration procedure is the same as that described for a single sample-and-hold system, with the following exceptions:

1. When adjusting for the 0000-to-0001 transition as described in Paragraph 4.2.3, use A406 potentiometer R27 for the coarse adjustment as before; however, use A406 potentiometer R28, rather than R16, for the fine adjustment.

2. With the EDC connected to channel 0, perform the 0000-to-0001 transition adjustments on A406 Sample-and-Hold module number 1, and the 7776-to-7777 transition adjustments on the A804 as described in step 5 of Paragraph 4.2.3.

3. With the EDC connected to channel 10_8 and the Switch register set to 000010_8, perform the 0000-to-0001 transition adjustments described in step 1 of Paragraph 4.2.3.

4. With the EDC connected to channel 10_8 and the EDC output voltage set at +0.75V for a system with preamplifiers, or set at +3.75V for a system without preamplifiers, the LED display should read 7000, with a ±2 tolerance. If this is not the case, perform the procedures described in steps 5 and 6, below.

5. Set the EDC voltage for +0.99625V for a system with preamplifiers or for +4.98125V for a system without preamplifiers.

6. Adjust A804 potentiometer R15 for both channel 0 and channel 10_8 as close as possible to the 7770-to-7771 transition.

Because of slight differences in gain between multiplexer/sample-and-hold number 1 and multiplexer/sample-and-hold number 2, it may be necessary to adjust for one channel high and the opposite channel low. For example, channel 0 may be at the 7767-to-7770 transition and channel 10_8 may be at the 7771-to-7772 transition. Optimum adjustment of A804 potentiometer R15 will result in channels 0 and 10_8 bracketing the 7770-to-7771 transition with equal and opposite errors.

4.2.5 Switch Gain Multiplexer Calibration

The A408 module contains three zero adjustments: RTO coarse, RTO fine, and RTI. The RTO (referred-to-output) pots should only be adjusted at a gain of 1 (channels 0–17), where amplifier output effects predominate. The RTI (referred-to-input) pot should only be adjusted at a gain of 64 (channels 60–77), where amplifier input effects predominate.

It is always preferable to perform the A408 adjustments on the A408T Tester. An A408 module which has been properly adjusted on the A408T Tester needs no further adjustment in a properly-adjusted LPS11. Adjustment of an A408 module in the LPS should only be done if an A408T Tester is not available. Adjustment of an A408 in an LPS should be done without pre-amps. If the LPS contains pre-amps, they should be temporarily replaced by jumper cards and reinstalled after A408 adjustments are completed. If calibration of the LPSAD-12 is in doubt, it should be checked before replacing the A407 multiplexer with the A408. In order to minimize the effects of noise, the RTI (G=64) adjustment should be done using the *LPS Diagnostic Repeatability Test,* with CPU front console switch 13 in the up position, so that the LPS LED's display the average value of each burst of 512 conversions. The RTO (G=1) adjustment may obtain its LED display using either the Repeatability Test with switch 13 up or the Calibration Test.

4.2.5.1 EDC Voltage Source Available

1. Connect EDC to channel 0 input for a 0–7 A408 or channel 10 input for a 10–17 A408 (10–17 A408 need not be adjusted except for a dual sample-and-hold configuration – LPSSH installed).

2. Set EDC voltage at +1.25 mV. Use the diagnostic to monitor channel 0 or 10 (G=1).

3. Set fine RTO pot (R24) near its center point.

4. Adjust coarse RTO pot (R25) for display as close as possible to the 4000/4001 (50-50) transition.

5. Adjust fine RTO pot (R24) for exact 4000/4001 (50-50) transition.

6. Disconnect EDC and use a shorting plug to force a zero input on channel 0 or 10.

7. Use the diagnostic to monitor channel 60 or 70 (G=64).

8. Set RTI pot (R22) for display of 4000.

9. Recheck channel 0 or 10 (G=1) and repeat if necessary.

4.2.5.2 EDC Not Available – If an EDC is not available, the channel 0 or 10 (G=1) adjustments should be performed using a shorting plug to force a zero input. In this case, the RTO pots should be adjusted for the middle of the 4000 output code instead of the 4000/4001 transition.

4.2.5.3 Pre-amp Adjustments with SG – The offset of the LPSAG and LPSAG-VG pre-amps is adjusted on the pre-amp module tester to a tolerance commensurate for use with the A407 Fixed Gain Multiplexer module (operating at a gain of 1). This can cause significant offsets on those channels for which pre-amps are installed, when the A408 multiplexer is operated at higher gains. For example, a 500 μV offset at the output of a pre-amp, while only 0.2 LSB at G=1, equals approximately $13_{10}=15_8$ LSB at G=64.

This offset should be adjusted out for each pre-amp channel, using the pre-amp balance adjust pot, while operating in the LPS. The channel input should be set to zero with a shorting plug. The LPS Diagnostic Repeatability Test should be run at G=64, with CPU front console switch 13 in the up position, so that the LPS LED's display the average value of each burst of 512_{10} conversions. The balance adjust pot should be set for a display of 4000.